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ANALYSIS AND DESIGN OF CMOS VOLTAGE-FOLDING CIRCUITS AND THEIR USE IN HIGH SPEED ADCS

by

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June 1996

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This thesis provides a complete numerical analysis of a complementary metal-oxide semiconductor (CMOS) analog folding circuit architecture, which is comprised of a number of parallel folding stages connected to an output stage. The bias point (reference voltage at which input signal is to be folded) and differential input responses are determined analytically. Current source requirements are also determined to ensure that the transistors remain in saturation. Using the analysis, a design process for implementing the folding circuit as a preprocessor for an analog-to-digital converter (ADC) is developed. A folding circuit preprocessor for a 6-bit optimum symmetrical number system (SNS) ADC is designed using this process. The designed circuit output is numerically analyzed and compared with HSPICE simulation results to verify the design process. Transfer function results are evaluated numerically to examine the preprocessor performance. Decimation bands are utilized within the ADC to eliminate coding errors. The effects of fabrication process tolerances, which alter the metal-oxide semiconductor field-effect transistor (MOSFET) parameters used in the analysis and design of the circuit, are quantified using a four-corner approach.

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ANALYSIS AND DESIGN OF CMOS VOLTAGE-FOLDING CIRCUITS AND THEIR USE IN HIGH SPEED ADCS

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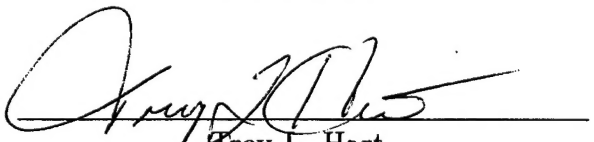
Author: 
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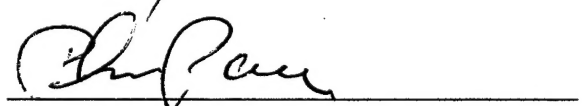
Approved by: 
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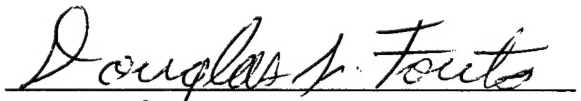
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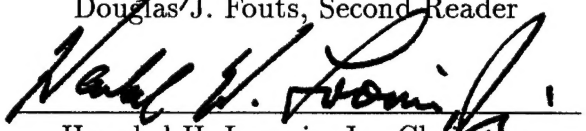
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I. INTRODUCTION

A. FOLDING CIRCUIT ANALOG-TO-DIGITAL CONVERTERS

Analog-to-digital converters (ADCs) are an integral part of many of the technological advances being made today. As a result, significant research is devoted to finding ways to make ADCs that are faster, smaller, more power efficient, and which produce less heat. The oldest and potentially the fastest method of conversion remains the flash ADC architecture which uses a parallel bank of comparators to amplitude-analyze the input signal. The large number of comparators required leads to increased size and power consumption. Efforts to maintain desirable performance characteristics while reducing the number of comparators required have produced many alternative approaches. The two-step flash ADC converter, which first performs a coarse quantization and then a fine quantization on the remaining portion of the signal, is one such approach. The major drawback to this approach is the synchronization of the coarse and fine outputs which creates a timing problem.

The use of *folding circuits* to fold the input signal (preprocessing) is another means to achieve these goals. Folding circuit preprocessors have been incorporated into ADCs in many different ways. The first architecture used a flash ADC to obtain the most significant bits (MSBs) and a parallel folding circuit ADC architecture to obtain the least significant bits (LSBs) [1]. An alternative to that approach incorporated Gray Coding into the folding circuit ADC for the LSBs [2,3]. The performance of folding circuits is degraded at higher frequencies as the tips of the folds start to round off creating non-linear regions where the comparators are not properly utilized. Double folding circuits which produce two folded waveforms differing only by a phase shift were investigated to reduce frequency limitations by ensuring that the peaks and valleys for one of the folds were within the linear region of the other fold at all times

[4]. To minimize frequency limitations, multiple folded waveforms, with no DC component, were considered. By amplitude-analyzing these about ground, the impact of the non-linear regions is minimized. A folding stage is required for each quantization level however, which provides no reduction in circuitry. A folding and interpolation architecture was introduced which reduced the number of folding stages required in this architecture by using interpolation between outputs of folding stages to generate additional folding signals [5,6]. The use of a symmetrical number system (SNS) as a preprocessing technique was then considered [7]. The SNS is used to decompose the amplitude analyzing operation into a number of sub-operations (moduli) which are of smaller computational complexity. Each sub-operation symmetrically folds the analog signal with a folding period equal to its modulus.[1] Since each sub-operation only requires precision in accordance with that modulus, a significant reduction in the number of comparators required is achieved. A much higher resolution is achieved by recombining the moduli. To further reduce the number of comparators within the SNS ADC, the optimum symmetrical number system, which is used in the preprocessing architecture design in this thesis, was defined. The optimum SNS considerably extends the dynamic range of the SNS ADC by redefining the moduli such that they produce a symmetrically folded waveform with a folding period equal to twice the modulus [8].

Complementary metal-oxide semiconductor (CMOS) devices have desirable performance characteristics, such as high gate impedances, lower power consumption, and design flexibility. Consequently, analog CMOS circuits that symmetrically fold an input signal are often used as preprocessors for high speed analog-to-digital converters [9,10]. The primary benefit of using CMOS folding circuit preprocessors in

[1] A brief example illustrating the operation of an SNS based ADC is given at the beginning of Chapter III.

an ADC is that they significantly reduce the number of comparators required to perform the quantization necessary for analog-to digital conversion. A straight $b = 6$ bit flash ADC, for example, requires $2^b - 1 = 63$ comparators to be loaded in parallel. By folding the input signal prior to quantization, the optimum symmetrical folding circuit ADC architecture requires only 15 comparators. By minimizing the number of comparators, a reduction in chip size, power consumption and heat dissipation is realized.

The CMOS folding circuit is composed of a number of folding stages interconnected in parallel. Each stage is also supplied with a reference voltage — the point at which the input signal is to be folded. The output stage consists of a summing amplifier, which combines the folding stage outputs into a single folded waveform, and a CMOS voltage-shifting arrangement. The output folding peaks and periods depend upon the transistor conductivity (a function of the device's gate lengths and widths), the current source values, bias voltages, and the frequency of the input signal. The analysis and design of the symmetrical folding circuit is critical to the performance of the preprocessor.

B. PRINCIPLE CONTRIBUTIONS

This thesis provides a thorough analysis of a CMOS analog folding circuit architecture. Previous work has examined several variations on this design using computer simulations from HSPICE, the industrial grade circuit analysis product from Meta-Software [11–13]. A detailed small signal analysis however, has not been completed. A CMOS folding circuit design process is described which provides a blueprint by which to adapt this architecture for specific preprocessing applications. The most sensitive components of the circuit design are identified and their parameters constrained to ensure proper operation of the circuit. The process outlined is proven by designing a

folding circuit preprocessor for a 6-bit SNS ADC architecture and implementing this design in HSPICE. The results of HSPICE simulations are compared with those from the analysis. Significant differences, most notably the capacitive effects on the folding circuit which are not accounted for in the analysis, are discussed and corrective measures are included.

The output of the newly designed analog folding circuit preprocessor is digitized using models of the comparator ladders and programmable logic arrays (PLAs) which comprise a SNS ADC architecture. The overall performance of the system is verified by observing its ADC transfer function response. Decimation bands are included to demonstrate their effectiveness in eliminating coding errors. The effects of fabrication process tolerances, which alter transistor parameters, are examined using a four-corner approach. These effects, most notably DC offset and waveform distortion, are shown to have a dramatic impact on the performance of the folding circuit preprocessor. Circuit design considerations to accommodate fabrication tolerances are discussed.

C. THESIS OUTLINE

This thesis begins with an overview of analog-to-digital converters and a brief discussion of previous techniques of incorporating folding circuit preprocessors into an ADC. The benefits of using CMOS folding circuits are discussed and a CMOS folding circuit is described.

In Chapter II, a mathematical analysis of the folding circuit, to include a single folding stage and the output stage, as well as the current source requirements is presented. A folding stage is represented in circuit form and shown to consist of two differential amplifier pairs, two active loads, a voltage-shifting arrangement and a source follower. The folding stages are connected in parallel to the output stage.

The output stage is comprised of a summing amplifier which is connected to another voltage shifting arrangement in order to achieve a folded output waveform in the desired voltage range. The analysis is compared with HSPICE simulation results to verify accuracy.

Chapter III opens with a presentation of the SNS ADC architecture and a discussion of the optimum SNS and its application in analog preprocessing. A preprocessor design approach is presented which provides a detailed method by which to incorporate the folding circuitry, analyzed in Chapter II, into a SNS architecture. A 6-bit optimum SNS folding circuit ADC preprocessor is designed using this outline. The designed preprocessor is simulated with HSPICE and the analysis is compared with HSPICE simulations results to verify the design process.

In Chapter IV, the 6-bit SNS folding circuit preprocessor output waveforms are applied to the SNS ADC, which is comprised of small comparator ladders and programmable logic arrays, to complete the conversion process. The overall ADC performance is obtained by observing the ADC transfer function response. The use of decimation bands to eliminate coding errors is discussed.

Chapter V investigates the effects of fabrication tolerances on circuit design and performance. The accuracy to which the designed folding circuit can be fabricated is shown to have significant effects on the performance of the folding circuit preprocessor. These effects, and possible corrective measures to account for them, are presented.

Finally, in Chapter VI, some concluding remarks are provided. Limitations of the CMOS voltage folding circuits as a preprocessor for ADCs are described and recommendations for further research are provided.

II. CMOS FOLDING CIRCUIT ANALYSIS

A. FOLDING STAGE

The function of each folding stage is to fold the input voltage at a particular reference voltage. A single folding stage is shown in Figure 1 and consists of two differential amplifier pairs (M3, M4 and M1, M2), two active loads (M5 and M6), a voltage level shifting arrangement (M7 and M8) and a source follower (M9) which ensures a low output resistance. The key to proper operation of the folding stage is for both differential amplifier pairs to remain in saturation throughout the entire input range. The following analysis assumes that all metal-oxide semiconductor field-effect transistor (MOSFET) pairs are perfectly balanced (i.e., the conductivity parameter K, and the threshold voltage V_T, for each transistor of the pair is the same) [14].

The analysis begins with an examination of the operation of the differential amplifier pairs. In general, differential amplifier pairs split between them the current required by the current source connected to their common sources. When there is no input differential ($V_{in} = V_{ref}$) then each MOSFET has a drain current equal to half the current source. When a differential exists, the MOSFET with the larger gate voltage carries a larger portion of the current up to the point where its drain current is equal to the current source and the other MOSFET of the pair has no drain current through it. The way that the current is switched based on the voltage differential is a function of the bias point (or quiescent point) gate to source voltage. To determine the operation of the differential amplifier pairs, the bias point operating parameters must be determined.

1. Bias Point Analysis

The input voltage, V_{in}, is applied to the gate of M3 of the lower differential amplifier pair. The bias (or quiescent) point of the lower differential pair (M3, M4)

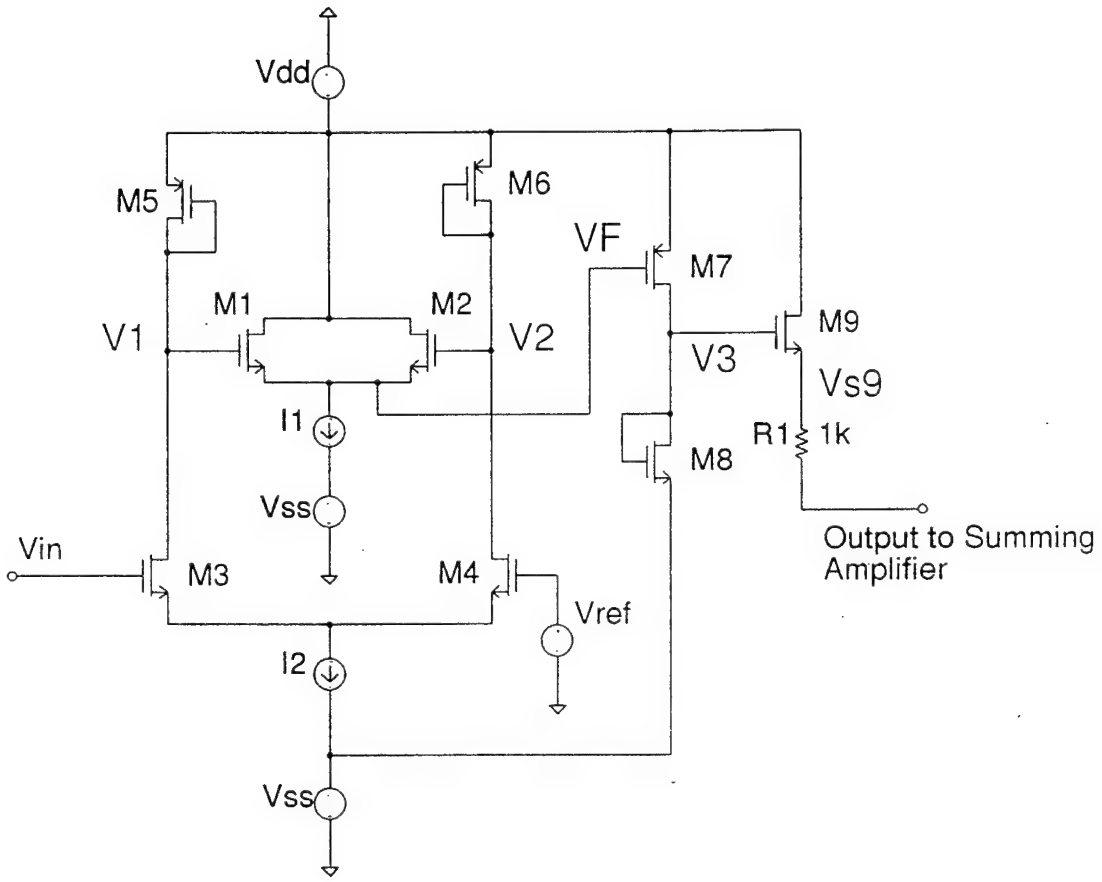

Figure 1: Single folding stage.

occurs when the gate voltages applied to the two transistors are equal ($V_{\text{in}} = V_{\text{ref}}$). At this point, the drain current, i_3 through M3 is equal to the drain current i_4 through M4. The total current through the two transistors must, at all times, equal the current source I_2, $i_3 = i_4 = I_2/2$. The gate to source voltage V_{gs} at the bias point can be determined from the standard equation for the operation of MOSFETs in the saturation region

$$I_d = K(V_{gs} - V_T)^2 \tag{1}$$

where I_d is the drain current. For transistors M3 and M4, the bias point gate-to-source voltages, which are equal and identified as V_{GS34}, can be determined as

$$V_{GS34} = V_{T34} + \sqrt{\frac{I_2}{2K_{34}}} \tag{2}$$

where K_{34} is the conductivity parameter for both M3 and M4 and V_{T34} is the threshold voltage for M3 and M4 (perfectly balanced pairs).

Because the current through each side of the differential pair is equal and the active loads M5 and M6 are assumed to be balanced (i.e., K_{56}, V_{T56}), the voltages applied to the gates of the upper differential pair M1, M2 are equal. Since M5 and M6 are by design always in saturation, the drain current through them is also defined by (1). With $V_{gs5} = V_1 - V_{dd}$ for M5 and $V_{gs6} = V_2 - V_{dd}$ for M6, and taking into account that for p-type (PFET) MOSFETs $V_{gs} - V_T$ is a negative voltage, it can be shown that

$$V_1 = V_2 = V_{dd} + V_{T56} - \sqrt{\frac{I_2}{2K_{56}}}\ . \tag{3}$$

Since the gate voltages applied to the two transistors M1 and M2 are equal, the bias point gate-to-source voltage V_{GS12} is also determined from (1) to be

$$V_{GS12} = V_{T12} + \sqrt{\frac{I_1}{2K_{12}}} \tag{4}$$

where I_1 is the current source for M1 and M2 and K_{12} is the conductivity parameter for both M1 and M2. The output voltage, V_F, at the bias point is equal to the source voltage of this differential pair. Since $V_{gs} = V_1 - V_F$, from (4) V_F is derived to be

$$V_F = V_1 - V_{T12} - \sqrt{\frac{I_1}{2K_{12}}} \tag{5}$$

which is the gate voltage of M7 at the bias point.

2. Differential Input Analysis

The results of applying a differential input to the lower differential amplifier (M3, M4) as would be common during normal operation of the circuit are now investigated. At the bias point $i_3 = i_4$. An input voltage differential $V_{id34} = V_{\text{in}} - V_{\text{ref}}$ creates an imbalance in the drain currents through M3 and M4. These currents, in turn, affect V_1 and V_2 separately to establish a second voltage differential $V_{id12} = V_1 - V_2$ which creates an imbalance in the drain currents through M1 and M2. The current imbalance produces different gate-to-source voltages V_{gs1} and V_{gs2} from which V_F can be determined.

Since M3 and M4 are balanced, the drain currents of M3 and M4 for a differential input are obtained from (1) as

$$i_3 = K_{34}(V_{gs3} - V_{T34})^2 \tag{6}$$

and

$$i_4 = K_{34}(V_{gs4} - V_{T34})^2 \ . \tag{7}$$

Subtracting (7) from (6) and substituting the differential voltage input, $V_{id34} = V_{g3} - V_{g4} = V_{gs3} - V_{gs4}$, it can be shown that

$$\sqrt{i_3} - \sqrt{i_4} = \sqrt{K_{34}}\, V_{id34} \ . \tag{8}$$

Combining (8) with the current source constraint that $i_3 + i_4 = I_2$ and solving simultaneously for i_3 and i_4 yields

$$i_3 = \frac{I_2}{2} + \sqrt{2K_{34}I_2}\left(\frac{V_{id34}}{2}\right)\sqrt{1 - \frac{\left(\frac{V_{id34}}{2}\right)^2}{\left(\frac{I_2}{2K_{34}}\right)}} \tag{9}$$

$$i_4 = \frac{I_2}{2} - \sqrt{2K_{34}I_2}\left(\frac{V_{id34}}{2}\right)\sqrt{1 - \frac{\left(\frac{V_{id34}}{2}\right)^2}{\left(\frac{I_2}{2K_{34}}\right)}} . \tag{10}$$

From (2) it can be seen that

$$\frac{I_2}{2} = K_{34}(V_{GS34} - V_{T34})^2 . \tag{11}$$

Using this relationship, (9) and (10) can be rewritten as

$$i_3 = \frac{I_2}{2} + \left(\frac{I_2}{V_{GS34} - V_{T34}}\right)\left(\frac{V_{id34}}{2}\right)\sqrt{1 - \left\{\frac{\left(\frac{V_{id34}}{2}\right)}{(V_{GS34} - V_{T34})}\right\}^2} \tag{12}$$

$$i_4 = \frac{I_2}{2} - \left(\frac{I_2}{V_{GS34} - V_{T34}}\right)\left(\frac{V_{id34}}{2}\right)\sqrt{1 - \left\{\frac{\left(\frac{V_{id34}}{2}\right)}{(V_{GS34} - V_{T34})}\right\}^2} . \tag{13}$$

From (12) and (13), the value of V_{id34} at which full switching occurs (i.e., the one MOSFET has a drain current equal to the current source and the other has no drain current) can be obtained. Setting i_3 in (12) equal to I_2 and solving for V_{id34} yields

$$\mid V_{id34} \mid_{max} = \sqrt{2}(V_{GS43} - V_{T34}). \tag{14}$$

The fold width, V_{fw}, achieved from this differential pair will be equal to twice the value of its maximum differential input voltage at full switching as seen by

$$V_{fw} = 2\sqrt{2}(V_{GS34} - V_{T34}). \tag{15}$$

Using (12) and (13), (1) can be applied to the active loads M5 and M6 to find the gate voltages, V_1 and V_2,

$$V_1 = V_{dd} + V_{T56} - \sqrt{\frac{i_3}{K_{56}}} \tag{16}$$

$$V_2 = V_{dd} + V_{T56} - \sqrt{\frac{i_4}{K_{56}}} \, . \tag{17}$$

The differential input to the upper amplifier M1, M2 is then

$$V_{id12} = V_1 - V_2 \, . \tag{18}$$

Following the same procedure used for the lower differential amplifier, the drain currents for each of the transistors in the upper differential amplifier can be obtained as

$$i_1 = \frac{I_1}{2} + \left(\frac{I_1}{V_{GS12} - V_{T12}}\right)\left(\frac{V_{id12}}{2}\right)\sqrt{1 - \left\{\frac{\left(\frac{V_{id12}}{2}\right)}{(V_{GS12} - V_{T12})}\right\}^2} \tag{19}$$

and

$$i_2 = \frac{I_1}{2} - \left(\frac{I_1}{V_{GS12} - V_{T12}}\right)\left(\frac{V_{id12}}{2}\right)\sqrt{1 - \left\{\frac{\left(\frac{V_{id12}}{2}\right)}{(V_{GS12} - V_{T12})}\right\}^2} \, . \tag{20}$$

With the drain currents for each transistor now known, the gate to source voltage for each transistor can be determined using (2). From the gate-to-source voltages of M1 and M2 the corresponding source voltages are found to be

$$V_{S1} = V_1 - V_{T12} - \sqrt{\frac{i_1}{K_{12}}} \tag{21}$$

and

$$V_{S2} = V_2 - V_{T12} - \sqrt{\frac{i_2}{K_{12}}} \, . \tag{22}$$

The folded voltage waveform V_F, that is forwarded to the voltage shifter, is the common source voltage of transistors M1 and M2. Therefore, V_F will be

$$V_F = \max(V_{S1}, V_{S2}) \, . \tag{23}$$

Note when $i_1 = i_2 = I_1/2$ (bias point), V_F is given by (5). V_F represents the input voltage folded at the reference voltage, V_{ref}, for one stage of the folding circuit as shown in Figure 2. Also shown for comparison are HSPICE simulation results. This folded waveform must now be processed so that it can be combined with the folded waveform from the other folding stages in the circuit. This is accomplished using an amplifier and voltage shifting arrangement followed by a source follower to ensure low output resistance to the summing amplifier.

Since the drain current through M7 is equal to the drain current through M8, using (5)

$$K_7(V_{gs7} - V_{T7})^2 = K_8(V_{gs8} - V_{T8})^2 \ . \tag{24}$$

Substituting $V_{gs7} = V_F - V_{dd}$ and $V_{gs8} = V_3 - V_{ss}$, (24) can be solved for V_3, the gate voltage to the source follower. In terms of the folded voltage V_F, V_3 can be expressed as

$$V_3 = \sqrt{\frac{K_7}{K_8}}(V_{dd} + V_{T7} - V_F) + V_{ss} + V_{T8} \ . \tag{25}$$

MOSFET parameters used in the simulations are shown in Table 1. It can be noted that the threshold voltages for M1, M2, M3, M4, and M9 are larger than the others. This is attributed to the body effect. The body effect is created by a reverse bias between the source and substrate (body) of a MOSFET [14]. The body is normally connected to the most negative power supply for n-type (NFET) MOSFET and the most positive power supply for PMOS to maintain a reverse bias. If the source of the MOSFET is not connected to the same supply, a reverse bias exists between the source and body, which widens the depletion region and reduces the channel depth. This results in V_{gs} having to be increased to produce the same drain current. This effect can be modeled as an increase in the threshold voltage, V_T, given by

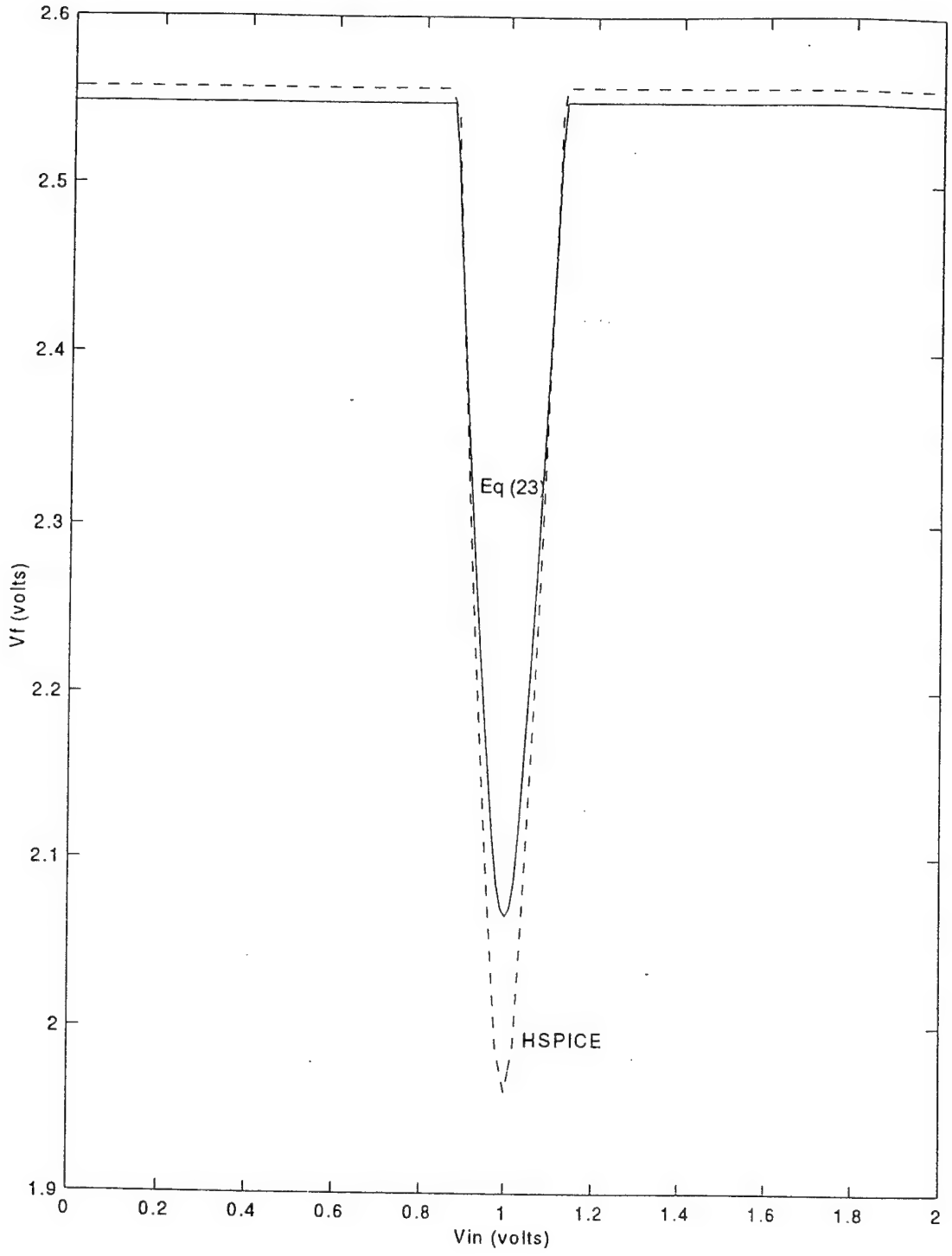

Figure 2: Comparison of folding voltages at node V_F.

Table 1: MOSFET Parameters Used in Single Folding-Stage Simulations

Transistors	$K\,(\mu A/V^2)$	V_T (V)	$\lambda\,(1/V)$
M1, M2	1683.3	1.53	—
M3, M4	3198.3	1.55	—
M5, M6	88.0	−0.75	—
M7	1188.5	−0.75	$-\frac{1}{7.5}$
M8	95.4	0.775	$\frac{1}{20}$
M9	196.4	1.82	—
M10	99.0	−0.75	$-\frac{1}{8.5}$
M11	117.8	0.775	$\frac{1}{16}$

$$V_T = V_{TO} + \gamma\left(\sqrt{\phi + V_{SB}} - \sqrt{\phi}\right) \tag{26}$$

where V_{T0} is the zero-bias threshold voltage, γ is the bulk threshold (process) parameter and ϕ is the surface potential at strong inversion, which is a physical parameter of the transistor. The source to body bias voltage is V_{SB}. Body effects are present in varying degrees in M1, M2, M3, M4, and M9 and are incorporated into the analysis by using (26) to increase the threshold voltages of these MOSFETs to improve comparison to HSPICE results.

Figure 3a shows V_3 (25) as a function of V_{in}. Comparison with HSPICE simulations reveals a significant discrepancy. This difference is attributed to channel length

modulation effects in M7 and M8. Channel length modulation occurs when the drain to source voltage increases above its saturation value [14]. This, in effect, shortens the channel length. Since the conductivity parameter K is inversely proportional to the channel length, this has the effect of increasing K, thereby increasing the drain current above the value expected for a given V_{gs}. This effect can be modeled by modifying (1) as

$$I_d = K(V_{gs} - V_T)^2(1 + \lambda V_{ds}) \tag{27}$$

where V_{ds} is the corresponding drain to source voltage and λ is the channel length modulation parameter. For a given MOSFET model, λ can be determined graphically from a current-voltage plot for several constant values of V_{gs} as shown in Figure 4. The straight line saturation characteristics, when extrapolated, intercept the V_{ds} axis at a common point $-V_A$. The parameter λ is the inverse of V_A. Applying (27) to M7 and M8 and equating (the drain currents through the two are equal), yields

$$K_7(V_F - V_{dd} - V_{T7})^2 \left[1 + \lambda_7(V_3 - V_{dd})\right] = K_8(V_3 - V_{ss} - V_{T8})^2 \left[1 + \lambda_8(V_3 - V_{ss})\right] \ . \tag{28}$$

While V_3 cannot be readily obtained in this form, it is logical to assume that the modulation effect due to V_3 is caused by its previous value. This allows the present value of V_3 to be separated out as

$$V_{3(j)} = \sqrt{\frac{K_7(V_F - V_{dd} - V_{T7})^2 \left[1 + \lambda_7(V_{3(j-1)} - V_{dd})\right]}{K_8 \left[1 + \lambda_8(V_{3(j-1)} - V_{ss})\right]}} + V_{ss} + V_{T8} \tag{29}$$

where $V_{3(j)}$ is the present value and $V_{3(j-1)}$ is its previous value and λ_7 and λ_8 are the channel length modulation parameters for M7 and M8, respectively. This yields a much more favorable comparison with HSPICE, as shown in Figure 3b.

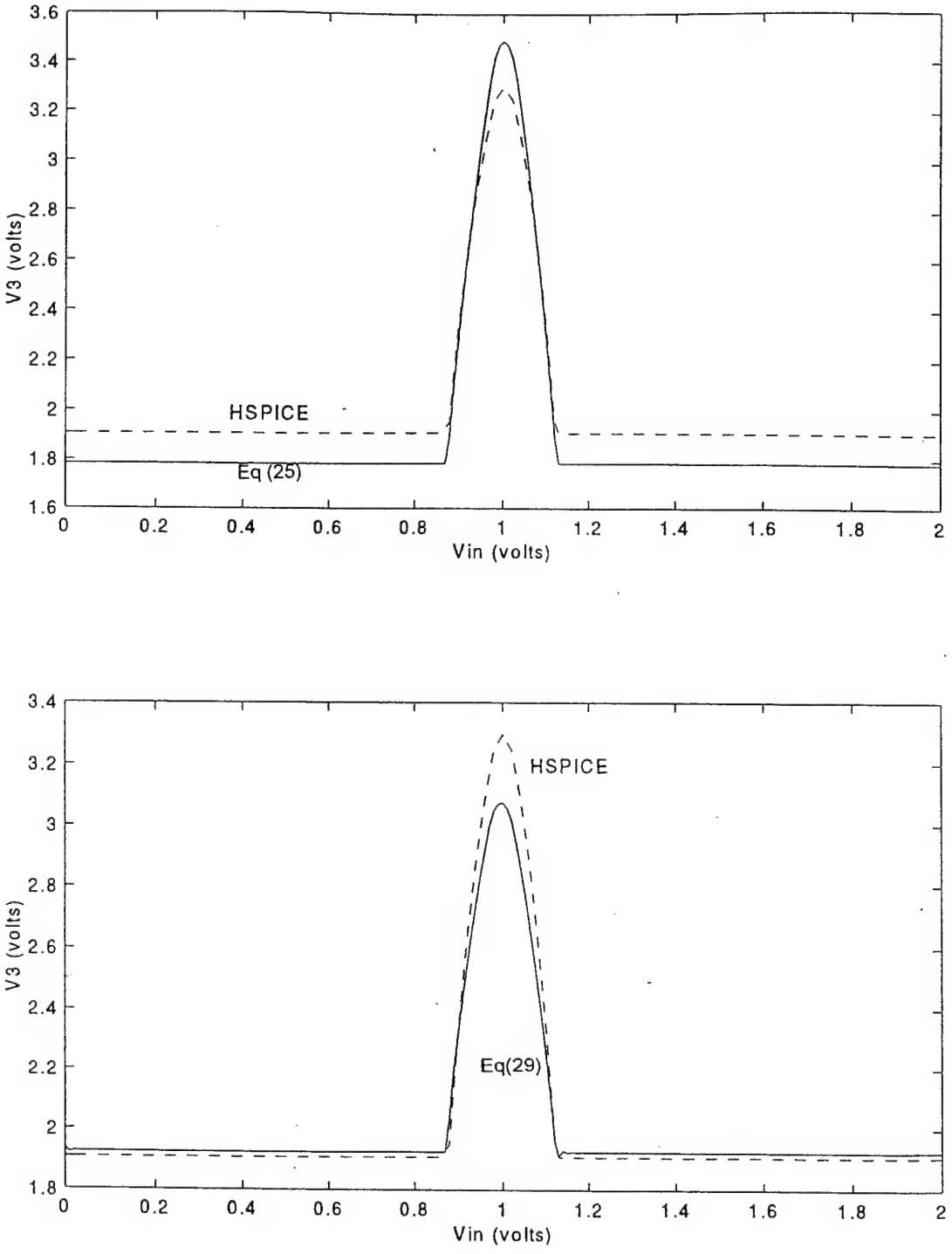

Figure 3: Comparison of folding voltages at node V_3. a) without channel length modulation parameter (25) and b) with channel length modulation (29).

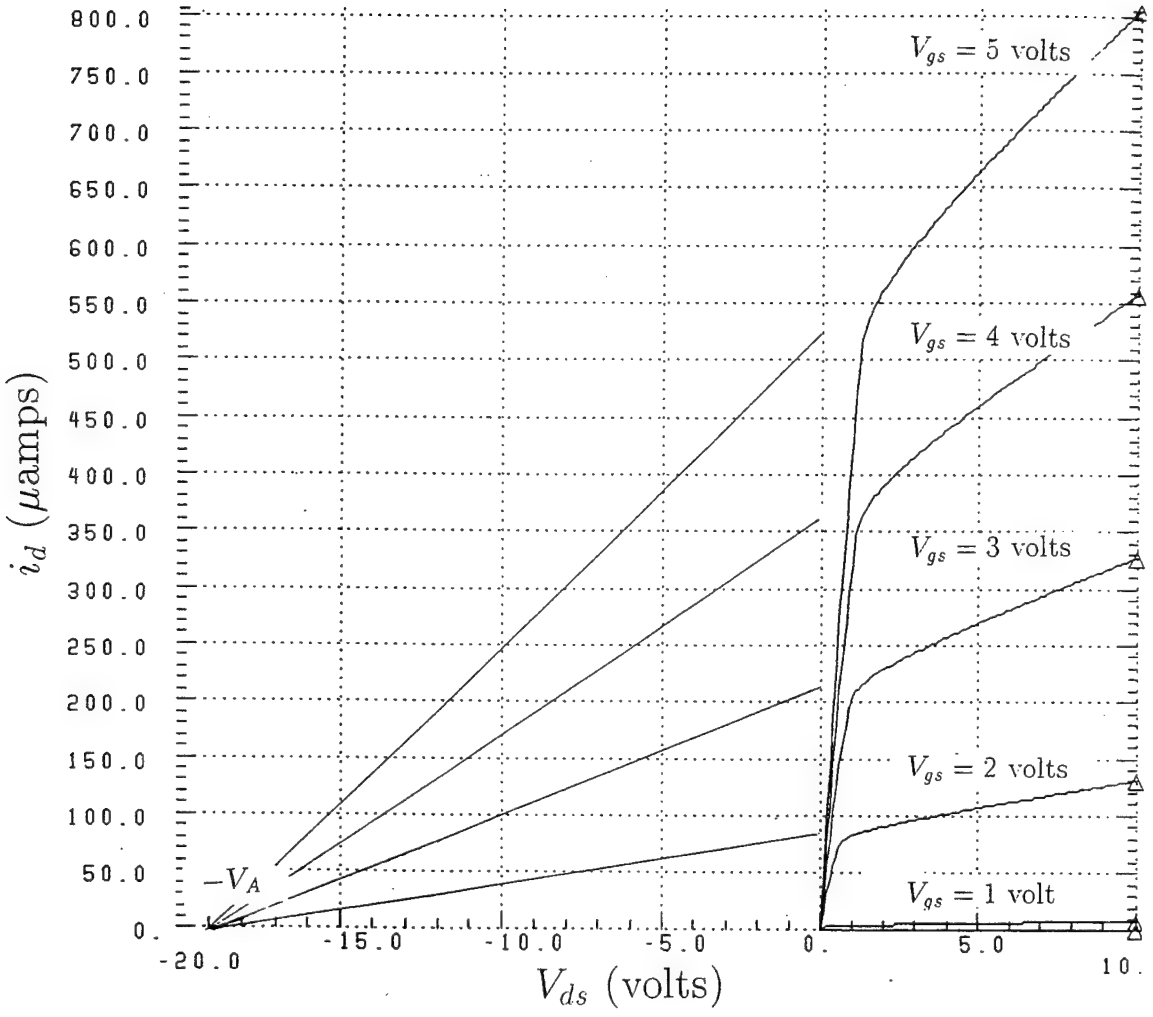

Figure 4: Voltage current curves to determine channel length modulation parameter λ.

In order to determine the drain current, i_9, through the source follower M9, the source voltage must be determined. Assuming that the operational amplifier that follows M9 is ideal and has no offset voltage, the voltage at the input of the operational amplifier (after the resistor R_1) should be zero volts. Using Ohm's law, the source voltage of M9, V_{S9}, is equal to the voltage drop across the 1 K ohm resistor (R_1). Since the drain current through M9 is equal to the current through R_1

$$V_{S9} = i_9 R_1 \ . \tag{30}$$

Combining (1) and (30) it is seen that

$$\frac{V_{S9}}{R_1} = K_9(V_3 - V_{S9} - V_{T9})^2 \tag{31}$$

which can be solved for V_{S9} in terms of the applied gate voltage V_3 as

$$V_{S9} = (V_3 - V_{T9}) + \frac{1}{2R_1K_9} - \frac{1}{2}\sqrt{\left[2(V_3 - V_{T9}) + \frac{1}{R_1K_9}\right]^2 - 4(V_3 - V_{T9})^2} \tag{32}$$

where V_{S9} represents the output voltage waveform for this single stage of the folding circuit (see Figure 1).

B. OUTPUT STAGE ANALYSIS

The folding circuit output summation stage consists of an inverting summing amplifier and a voltage shifter as shown in Figure 5. The input to the summing operational amplifier will be the composite sum of the voltage waveforms from each of the N different folding stages required to support its channel of the ADC. The summing configuration of the operational amplifier produces an output of

$$V_4 = -\left(\frac{R_f}{R_1}\right)(V_{S1} + V_{S2} + \cdots + V_{SN}) \tag{33}$$

where V_4 is the output of the operational amplifier and V_{S1} to V_{SN} are the source voltages of M9 for each of the N different folding stages connected to the input of

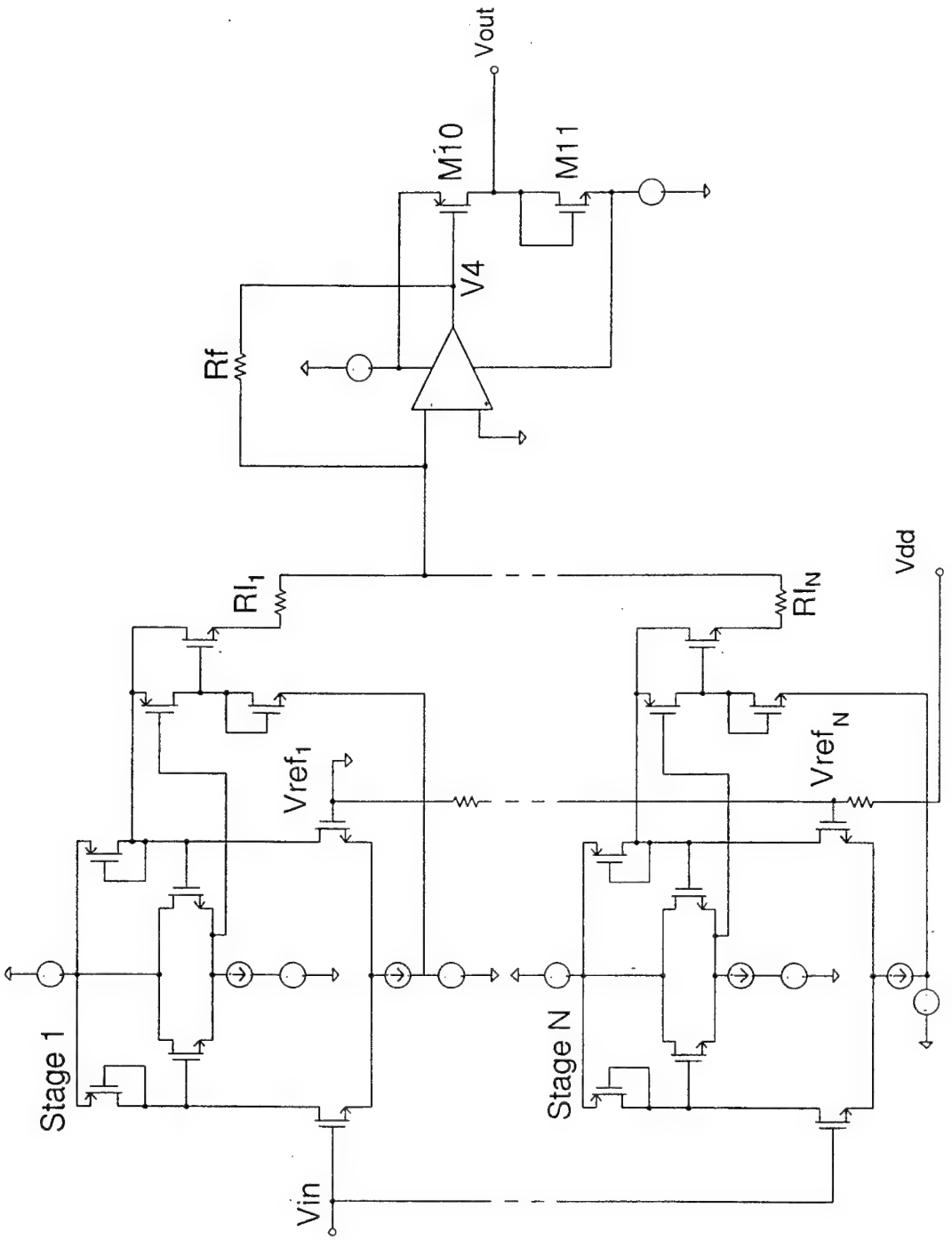

Figure 5: Complete folding circuit.

the operational amplifier. V_4 is then applied to the gate of M10 in the final voltage shifter of the output stage. Since the drain currents i_{10} and i_{11}, through M10 and M11, respectively, are equal, applying (1) with the substitutions $V_{gs10} = V_4 - V_{dd}$ and $V_{gs11} = V_{\text{out}} - V_{ss}$, it can be shown that

$$K_{10}(V_4 - V_{dd} - V_{T10})^2 = K_{11}(V_{\text{out}} - V_{ss} - V_{T11})^2 \tag{34}$$

from which it can be shown that

$$V_{\text{out}} = \sqrt{\frac{K_{10}}{K_{11}}}\,(V_{\text{dd}} + V_{T10} - V_4) + V_{ss} + V_{T11} \tag{35}$$

where V_4 is a function of the input voltage being folded. Figure 6a shows V_{out} as a function of the input voltage. Comparison with HSPICE shows a similar discrepancy to that of V_3. This again is attributed to channel length modulation effects. Applying the same analysis to M10 and M11 yields

$$V_{\text{out}(j)} = \sqrt{\frac{K_{10}(V_4 - V_{dd} - V_{T10})^2\left[1 + \lambda_{10}(V_{\text{out}(j-1)} - V_{dd})\right]}{K_{11}\left[1 + \lambda_{11}(V_{\text{out}(j-1)} - V_{ss})\right]}} + V_{ss} + V_{T11} \tag{36}$$

As shown in Figure 6b, this yields a much more favorable comparison.

C. CURRENT SOURCE ANALYSIS

In order for the folding circuit to operate properly, both differential pairs must remain in the saturation region throughout the entire range of operation. In the saturation region of an NFET transistor, the drain-to-source voltage, V_{ds}, must be larger than the gate-to-source voltage minus its threshold voltage as

$$V_{ds} \geq V_{gs} - V_T\ . \tag{37}$$

Beginning with a bias point analysis of the lower differential pair (M3, M4), and limiting the analysis to only one transistor since they are balanced, $V_{ds} = V_1 - V_S$,

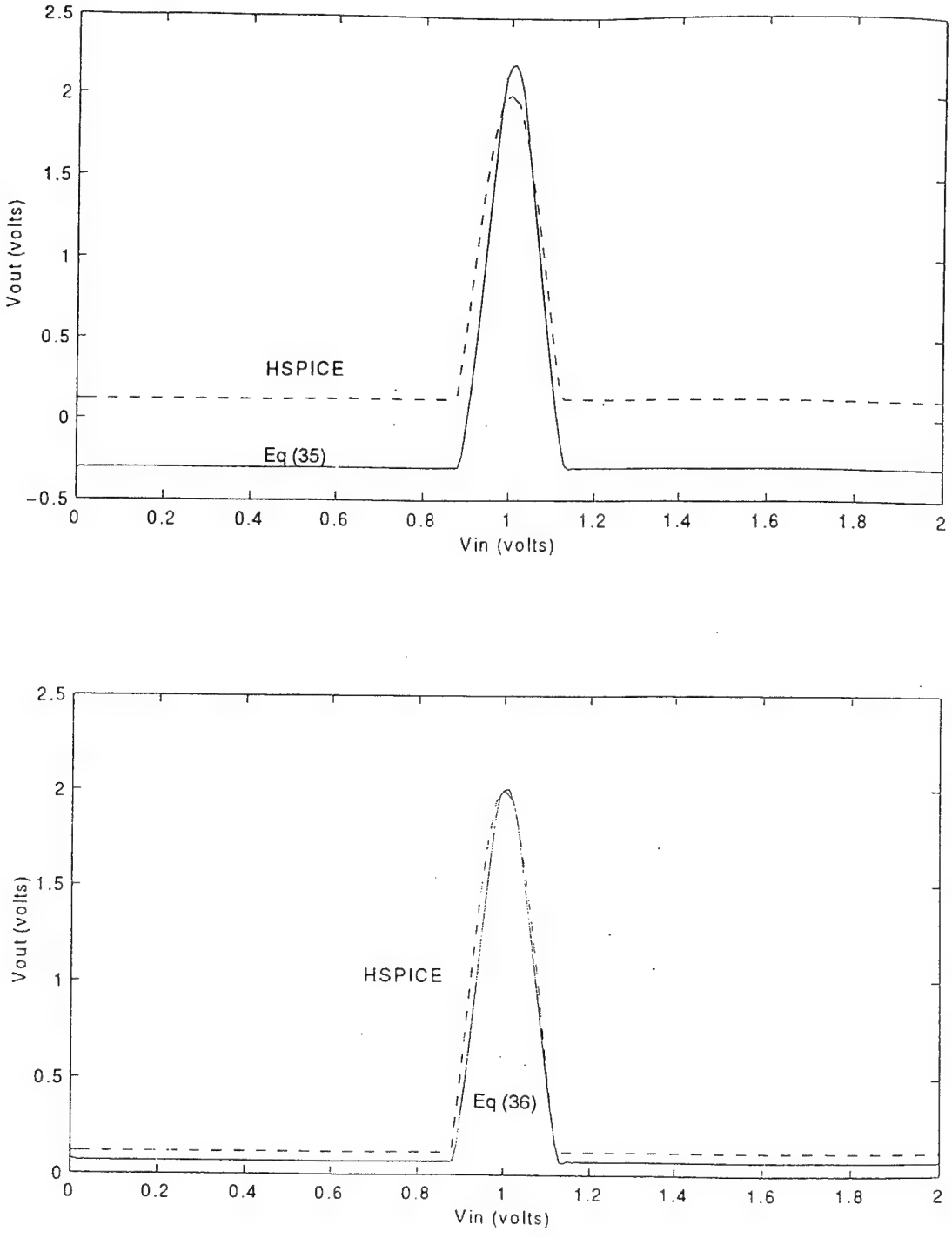

Figure 6: HSPICE comparison of output voltage at node V_{out}. a) without channel length modulation (35) and b) with channel length modulation (36).

and $V_{gs} = V_{\text{in}} - V_S$. Substituting these relationships into (37) and simplifying, the requirement for saturation is reduced to

$$V_1 \geq V_{\text{in}} - V_{T3} \ . \tag{38}$$

Substituting the relationship for V_1 in terms of I_2 derived in (3) this becomes

$$I_2 \leq 2K_{56}(V_{dd} + V_{T56} + V_{T34} - V_{\text{in}})^2 \ . \tag{39}$$

Similar results are obtained for M2 by replacing V_{in} with V_{ref}. Since I_2 is the same for every folding stage, it is clear that the limiting value for I_2 will occur for the folding stage has a bias point $V_{\text{in}} = V_{\text{ref}} = V_{\text{max}}$, where V_{max} is the maximum input voltage. At this point (39) becomes

$$I_2 \leq 2K_{56}(V_{dd} + V_{T56} + V_{T34} - V_{\text{max}})^2 \ . \tag{40}$$

The constraint imposed in (40) ensures that operation at the bias point is in the saturation region. To ensure that the lower differential pair remains in saturation throughout the entire range of operation, we apply the constraint of (38) along with the equation for V_1 in terms of the current i_3 (16) to get

$$i_3 \leq K_{56}(V_{dd} + V_{T56} + V_{T34} - V_{\text{in}})^2 \ . \tag{41}$$

For V_{in} larger than V_{ref} by more than half the folding width of the circuit, M3 will carry all the current and i_3 will be equal to the current source I_2. The maximum constraint will therefore be imposed when $V_{\text{in}} = V_{\text{max}}$ or

$$I_2 \leq K_5(V_{dd} + V_{T56} + V_{T34} - V_{\text{max}})^2 \ . \tag{42}$$

Since this constraint is more stringent than that imposed by (40), (42) should be used as the maximum value of I_2.

To examine the upper differential pair, we apply (37) with $V_{ds} = V_{dd} - V_S$ and $V_{gs} = V_1 - V_S$, it is seen that

$$V_{dd} \geq V_1 - V_{T1} \ . \tag{43}$$

By observation, it is clear that since V_1 is always less than V_{dd} and the threshold voltage for an NFET transistor is a positive value, this condition is always satisfied. Therefore, any current source will maintain the upper differential pair in the saturation region. The magnitude of the current source will only affect the voltage level of the folded output. For ease of design and fabrication, I_1 can be equal to I_2.

III. CMOS SNS PREPROCESSING

A. OPTIMAL SYMMETRICAL NUMBER SYSTEM

The folding circuit architecture used in this thesis implements the optimum symmetrical number system (SNS) [8]. The optimum SNS is composed of a number of pairwise relatively prime (PRP) moduli, m_i. Each SNS moduli contains a unique set of integers which are derived from a symmetrically folded waveform with a period equal to twice the PRP modulus. For a given modulus, m, the integer values are given by the row vector

$$x_m = [0, 1, .., m-1, m-1, .., 1, 0]. \tag{44}$$

Using this definition, a modulus 5 set, for example, would be [0,1,2,3,4,4,3,2,1,0].

Due to the presence of ambiguities within a modulus, a single modulus does not form a complete system of length $2m$ by itself. These ambiguities are resolved by considering N different PRP moduli together. By combining the N different channels, the SNS produces a complete system having a one-to-one correspondence with the residue number system. The dynamic range, M, of this system is equal to the product of the N different moduli

$$M = \prod_{i=1}^{N} m_i. \tag{45}$$

The dynamic range is also the position of the first repetitive moduli vector. For example, in an optimum SNS system with $m_1 = 3$ and $m_2 = 4$, the first repetitive moduli vector occurs at an input of 12, as shown in Table 2.

B. OVERVIEW OF SNS FOLDING ADC PREPROCESSING

In optimum SNS analog preprocessing, a system is constructed based on N different moduli (channels) that together produce the desired dynamic range. The architecture examined for this thesis employs the optimum SNS encoding scheme

Table 2: Optimum SNS Preprocessing

Normalized Input	SNS Moduli	
	3	**4**
0	0	0
1	1	1
2	2	2
3	2	3
4	1	3
5	0	2
6	0	1
7	1	0
8	2	0
9	2	1
10	1	2
11	0	3
12	0	3
Dynamic Range	$M = 12$	

using three parallel channels. To provide b-bit resolution, a dynamic range, M, of 2^b is required. The moduli, m_1, m_2, and m_3, chosen for the system must provide a dynamic range that is greater than or equal to M.

Figure 7 shows a block diagram of a SNS folding ADC. The input signal is applied to each channel in parallel. Each channel is composed of a number of folding stages. Every folding stage within a particular channel folds the input signal at a different reference voltage with a period of twice the modulus. The number of folding stages required per channel is a function of the fold width associated with each modulus. The fold width, V_{fw}, for a given modulus, m_i, is given by

$$V_{fw} = \frac{2m_i V}{M} \tag{46}$$

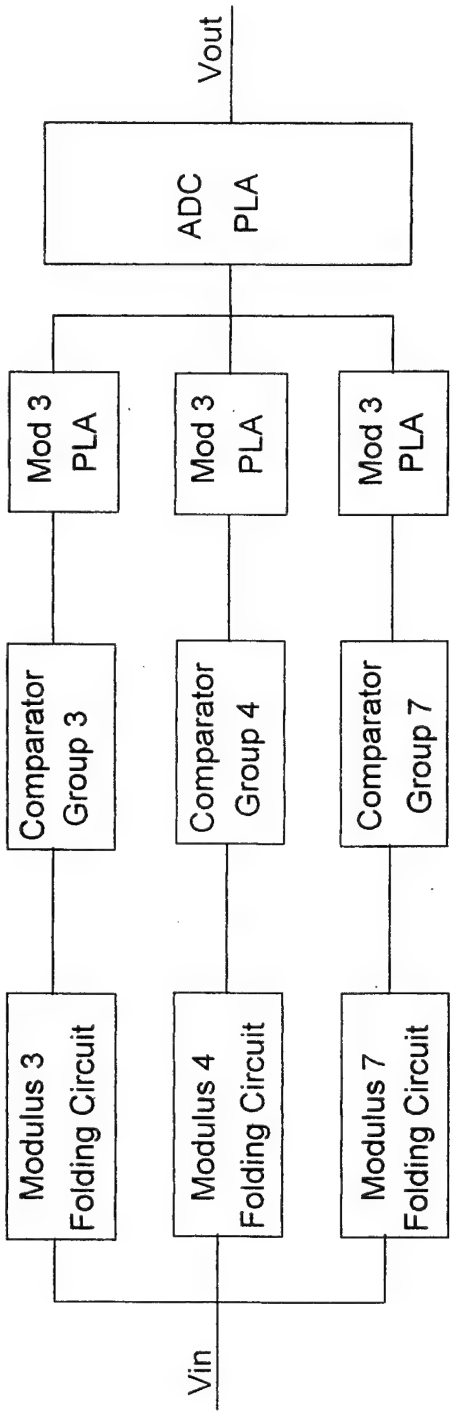

Figure 7: SNS ADC block diagram.

where V is the maximum input voltage and M is the desired dynamic range of the system. With the folding widths for each modulus determined, the number of folding stages, N_{fs}, required per channel is obtained from

$$N_{fs} = \frac{V}{V_{fw}} + 1 \tag{47}$$

where N_{fs} is rounded up to the next integer value.

Folding the input signal effectively increases the frequency of the input signal by a factor of N_{fs}. Figure 8 shows the HSPICE frequency response for frequencies ranging from 10 KHz to 1 MHz. This illustrates one of the major limitations of using folding circuit preprocessors. As the frequency increases, the folding peaks tend to round off and the peak-to-peak amplitude decreases. These effects are considerable at frequencies above 100 KHz. In an ADC, these effects render the comparators that analyze the peak regions unusable, resulting in missing codes [15].

The N_{fs} folding stage outputs are combined to form a single continuously-folded output waveform for each channel. This output waveform is mid-level quantized using a small comparator ladder consisting of $m_i - 1$ comparators. A channel PLA or similar device, is used to encode the comparator thermometer code for that channel. The outputs of each channel PLA, represent the thermometer code in a binary format and are recombined in a final PLA. The final PLA transforms the SNS format into a more convenient digital output.

C. PREPROCESSOR DESIGN OUTLINE

Using the folding circuit analysis in Chapter II and the description of the optimum SNS scheme presented above, a process by which to adapt the folding circuits to different specifications is developed. As an example, a three-channel, 6-bit CMOS folding circuit preprocessor for an SNS ADC architecture which uses ± 5 volt power

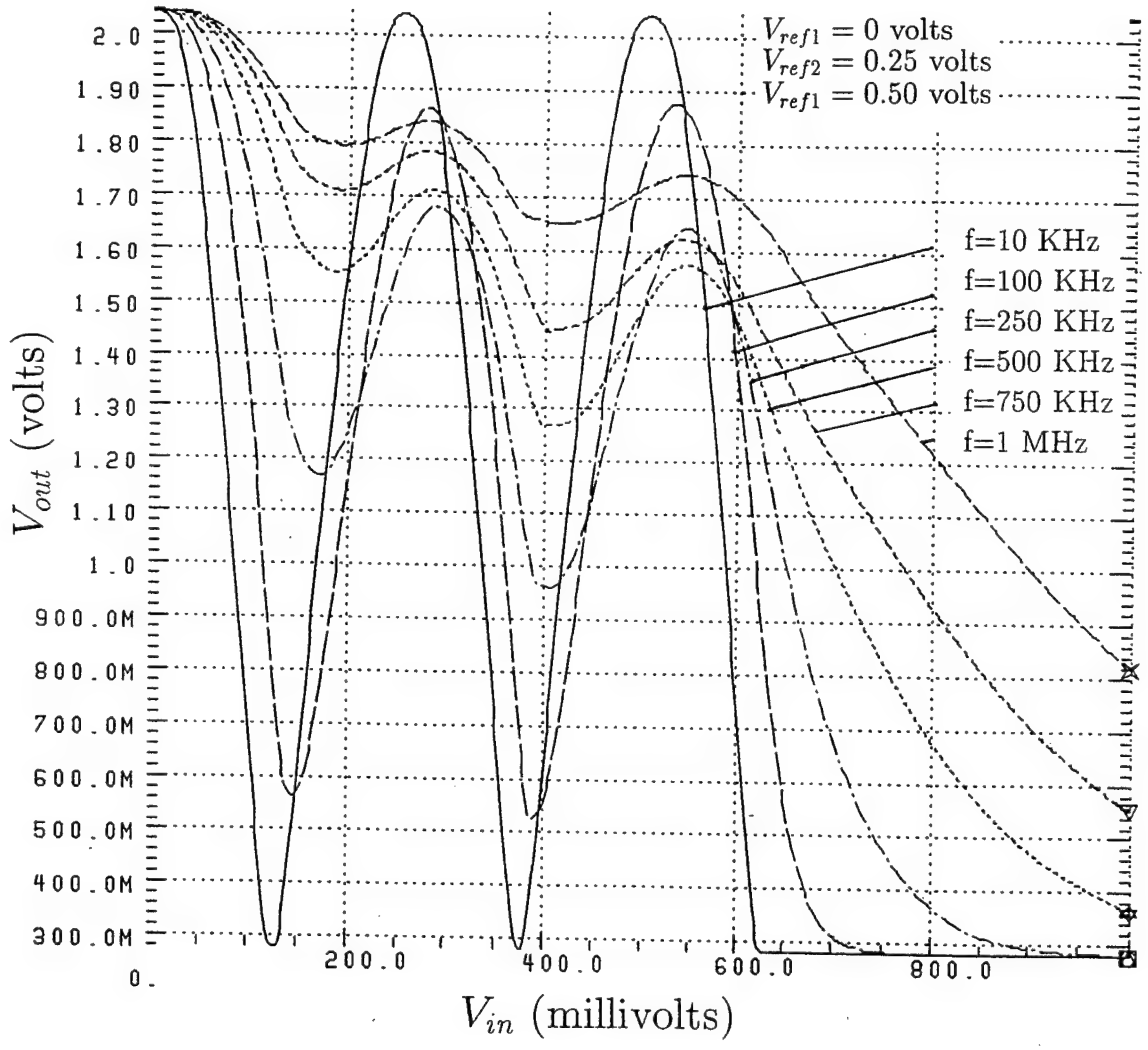

Figure 8: Folding circuit frequency response.

supplies common in today's computer and communications technology is designed. The considerations and limitations of the system design process are detailed.

The initial system specifications required before beginning the circuit design are bit accuracy and the maximum input voltage. The 6-bit SNS ADC is designed for a maximum input voltage of 3 volts. The bit accuracy is used to determine the minimum required dynamic range, M, of the system where $M = 2^6 = 64$. The PRP moduli are chosen ensuring that, from (45), the dynamic range achieved is greater than or equal to M. The selected moduli are $m_1 = 3$, $m_2 = 4$, and $m_3 = 7$. This combination produces a dynamic range of 84 which is sufficient to achieve the bit accuracy desired. With the moduli determined, the folding widths for each channel are obtained from (46) as

$$\text{Mod 3: } V_{fw} = 0.281 \text{ volts}$$
$$\text{Mod 4: } V_{fw} = 0.375 \text{ volts}$$
$$\text{Mod 7: } V_{fw} = 0.656 \text{ volts.}$$

By combining (11) and (15), the ratio of the current source I_2 to K_{34} is obtained for each channel by

$$V_{fw} = 2\sqrt{\frac{I_2}{K_{34}}}. \tag{48}$$

From (48), as the current source value increases, K_{34} must also increase to obtain the required folding widths. In general, the frequency response of a MOSFET degrades as the gate width (K value) of the transistor increases. To minimize this effect, it is advantageous to select the minimum practical value of I_2. For simplicity of design and analysis, the current sources, I_1 and I_2, are set equal to each other with a value of 100 μA. Rewriting (48) as

$$K_{34} = \frac{4I_2}{V_{fw}^2} \tag{49}$$

the lower differential amplifier transconductance parameters for each channel are determined to be

$$\begin{aligned} \text{Mod3}: \quad K_{34} &= 5065.8\mu\text{A}v^{-2} \\ \text{Mod4}: \quad K_{34} &= 2844.4\mu\text{A}v^{-2} \\ \text{Mod7}: \quad K_{34} &= 929.5\mu\text{A}v^{-2}\ . \end{aligned}$$

From (16) and (17), the active loads, M5 and M6, determine the magnitude of the maximum differential input to the upper differential amplifier pair of M1 and M2. From (18), it is observed that as the values of K_{56} decrease, the maximum differential input voltage is increased. A larger differential input voltage to the upper differential pair produces a sharper fold in the voltage waveform. The value selected for K_{56} must be large enough, however, to ensure that, from (42), the lower differential amplifiers will remain in the saturation region. Using the zero-bias threshold voltages for the MOSFET models (a conservative approach since the actual threshold voltage V_{T34} is increased by the body effect) K_{56} is chosen to be $20\mu\text{A}v^{-2}$.

The transconductance parameters K_{12} are chosen to be as large as practical to minimize the folding width of the upper differential amplifier which produces a less rounded waveform at the bias point. To maximize performance and keep K_{12} the same for all three channels, K_{12} is chosen to be similar in magnitude to the previously determined value of K_{34} for the highest modulus channel, in this circuit that of modulus 7. This prevents M1 and M2 from introducing any additional frequency limitations on the circuit. Accordingly, K_{12} are chosen to be $900\mu\text{A}v^{-2}$. At this point in the design process, it is practical to plot the folded output waveform, V_F, for a single fold. Figure 9 shows V_F for a single fold of the modulus 4 channel. From Figure 9, the folding width is verified to be correct and the minimum and maximum voltages to be forwarded to the voltage shifting arrangement of M7 and M8 are determined.

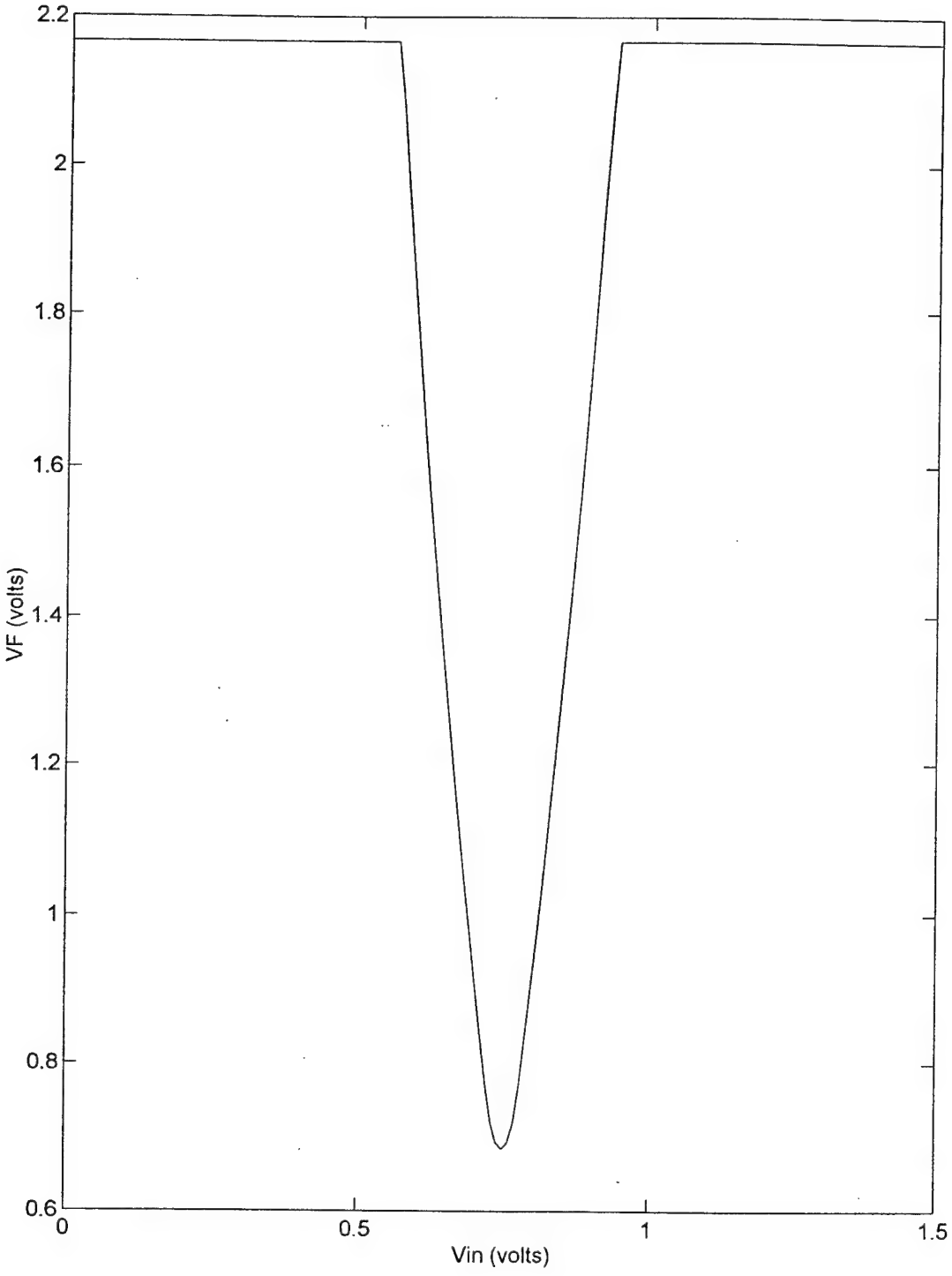

Figure 9: Folding voltage at node V_F for 6-bit circuit.

The values of K_7 and K_8 are critical to the proper operation of the circuit. The maximum value of V_F, which occurs outside of the fold width, is used to determine the ratio of K_7 to K_8. The lower limit for the ratio of K_7 to K_8 is obtained from the requirements for M9. From the perspective of M9, its gate to source voltage must be larger than its threshold voltage for the transistor to be turned on. When the input voltage is not within the folding range for that stage, it is desirable, for loading feedback and power considerations, that the voltage at the source of M9 be nearly zero volts. This occurs when the current through M9 is equal to zero. Combining these requirements, it is determined from (1) that $V_3 \geq V_{T9}$. This provides the lower limit for V_3 which is obtained when V_F is at its maximum value. Applying these constraints, the ratio of the values for K_7 and K_8 is determined from (25) or (29). For the system being designed, with the maximum value of $V_F = 2.2$, $V_{T9} = 1.55$, and $V_{T12} = 1.7$, the ratio of 8 is determined. The transconductance K_7 is chosen to be $800\mu\text{A}v^{-2}$ and K_8 is chosen to be $100\mu\text{A}v^{-2}$.

The value of K_9 determines the amount of current provided to the summing operational amplifier. For an input voltage outside the folding range of that particular folding stage, the current through M9 should ideally be equal to zero. At the folding reference voltage, the current will be at a maximum value which is determined by the value of K_9. From (30), the current through M9 determines the voltage, V_{S9}, applied to the summing operational amplifier from that particular stage. From (33), V_{S9} is multiplied by the value of the feedback resistor, R_F, of the operational amplifier. Therefore, the value of K_9 is kept small to ensure minimal current is drawn. This minimizes potential loading problems at the common connection between folding stages at the input of the summing operational amplifier and minimizes power consumption. The feedback resistor of the operational amplifier is used to scale the

signals as required to achieve the desired signal range entering the final voltage shifter. For this circuit, K_9 is chosen to be $10\mu \mathrm{A}v^{-2}$ and R_F is set to 20 Kohms.

The final step in the design is to determine the ratio of K_{10} to K_{11} in the final voltage shifter. It is beneficial to plot the input voltage, V_4, to the voltage shifter as shown in Figure 10. To optimize circuit performance, the ratio of K_{10} to K_{11} is chosen so that at the maximum input voltage to the shifter the output is ideally zero volts. From Figure 10, it is shown that the maximum value of $V_4 = 0$ volts. Applying this constraint to (36), a ratio of .9 is obtained from which K_{10} is chosen to $90\mu \mathrm{A}v^{-2}$ and K_{11} is chosen to be $100\mu \mathrm{A}v^{-2}$.

Table 3 provides a synopsis of the steps outlined above and identifies the applicable equation numbers as well as other conditions considered when determining each parameter value. Figure 11 shows the simulated output waveform for all three channels based on the numerical analysis. Table 4 provides a complete listing of all the MOSFET parameters for the newly designed 6-bit SNS Folding ADC. Table 5 describes the effects of circuit parameter modifications on the folded output voltage waveform. Appendix A provides the MATLAB m-file used to perform the numerical analysis. Appendix B provides the HSPICE models used to simulate the designed preprocessor.

Comparison with HSPICE simulation results for the modulus 7 output are shown in Figure 12 and reveal a variance in the widths of each fold as evident by the flat portions at the bottoms of the folds. This is due to capacitive effects in the circuit which are not accounted for in the numerical analysis but which are to be expected [11,12]. To compensate for these capacitive effects, the transconductance of the lower differential pair, (K_{34}), must be increased for each successive folding stage in order to obtain the proper folding widths. The transconductance of M3 and M4 were modified in HSPICE by trial and error until the fold widths were correct as shown in

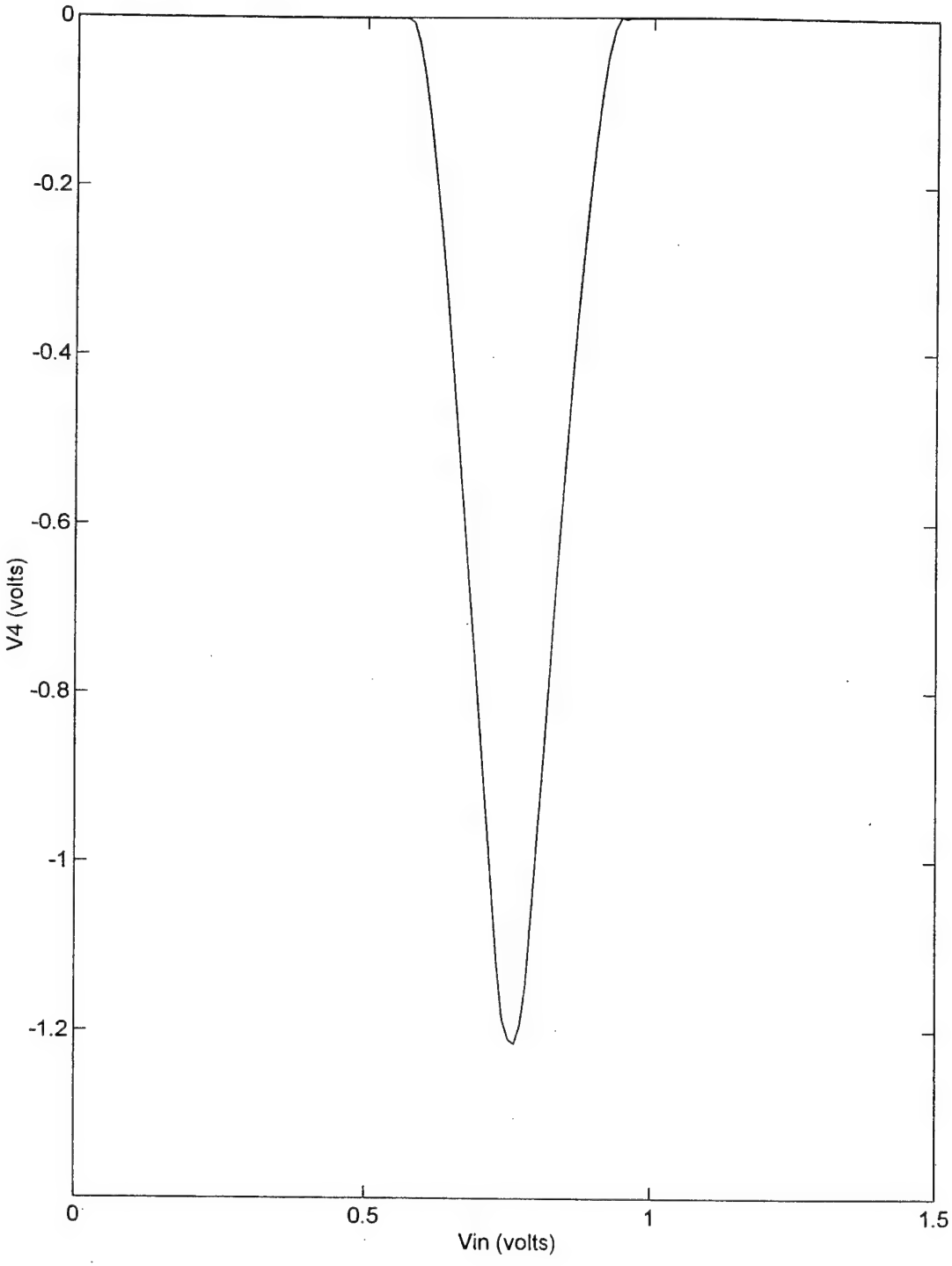

Figure 10: Folding voltage V_4 for 6-bit circuit.

Table 3: Preprocessor Design Outline

For a given system bit accuracy (b) and maximum input voltage V			
Step	**Variable to be determined**	**Governing Equation**	**Other Conditions**
1	Moduli $m_i \cdots m_N$	45	$\prod_{i=1}^{N} m_i > 2^b$
2	Folding widths V_{fwi}	46	
3	I_1, I_2	42	Minimize
4	K_3, K_4	49	
5	K_5, K_6	42	Minimize
6	K_1, K_2	—	Maximize, $\approx K_{34}$ min
7	K_7, K_8	25 or 29	$V_3 \geq V_{T9}$
8	K_9	30, 31	Minimize
9	R_F	33	
10	K_{10}, K_{11}	35 or 36	V_{out} min ≈ 0

Table 4: MOSFET Parameters for 6-Bit SNS ADC Simulations

Transistors	$K\,(\mu A/V^2)$	$V_T(V)$	$\lambda\,(1/V)$
M_1, M_2	900	1.75	—
M_3, M_4	Mod 3: 5065.8 Mod 4: 2844.4 Mod 7: 929.5	1.40	—
M_5, M_6	20	−0.75	—
M_7	800	−0.75	−1/10
M_8	100	0.75	1/15
M_9	10	1.55	—
M_{10}	100	0.75	−1/10
M_{11}	100	0.75	1/15

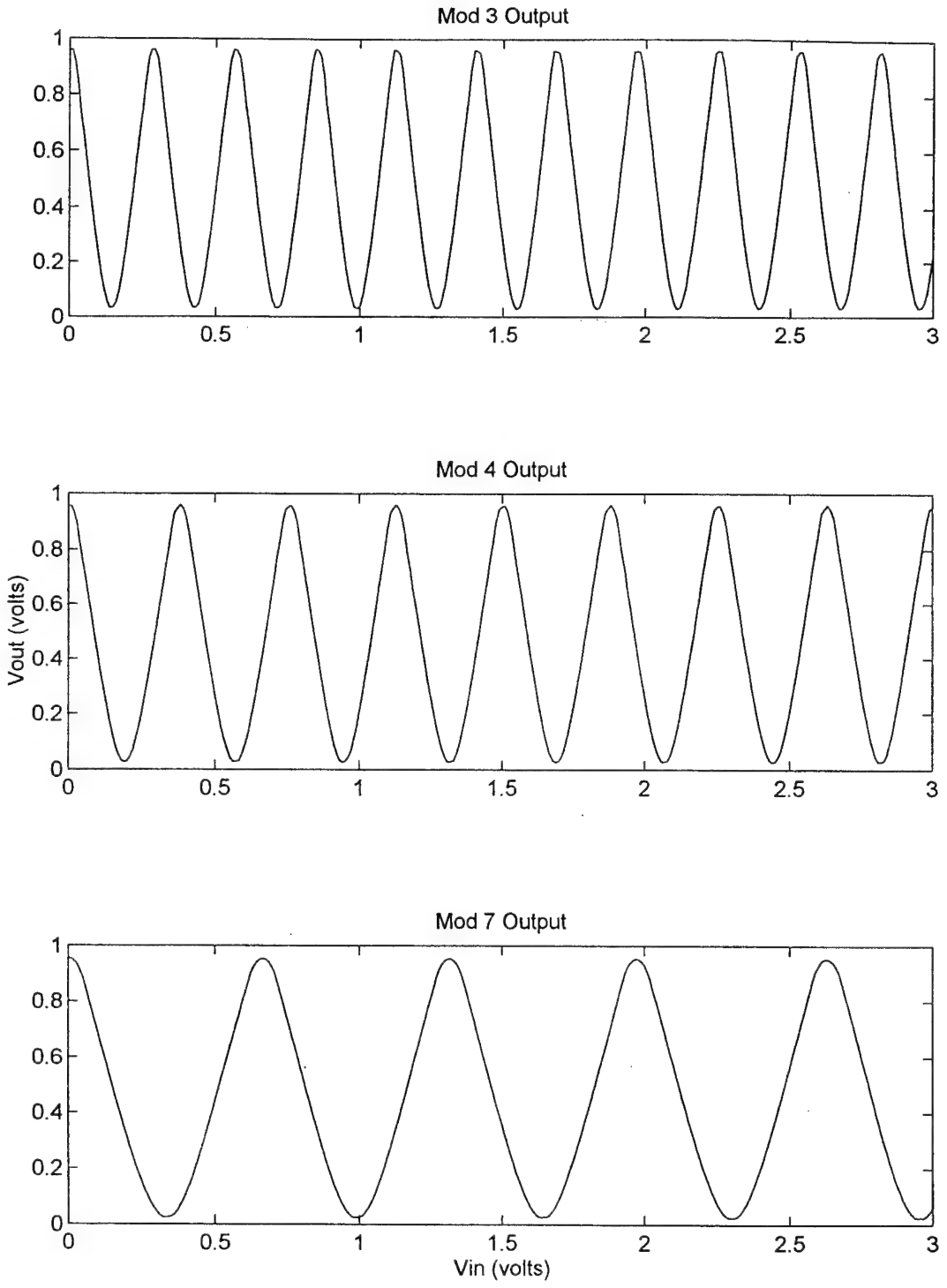

Figure 11: Folding circuit outputs for each modulus of 6-bit circuit.

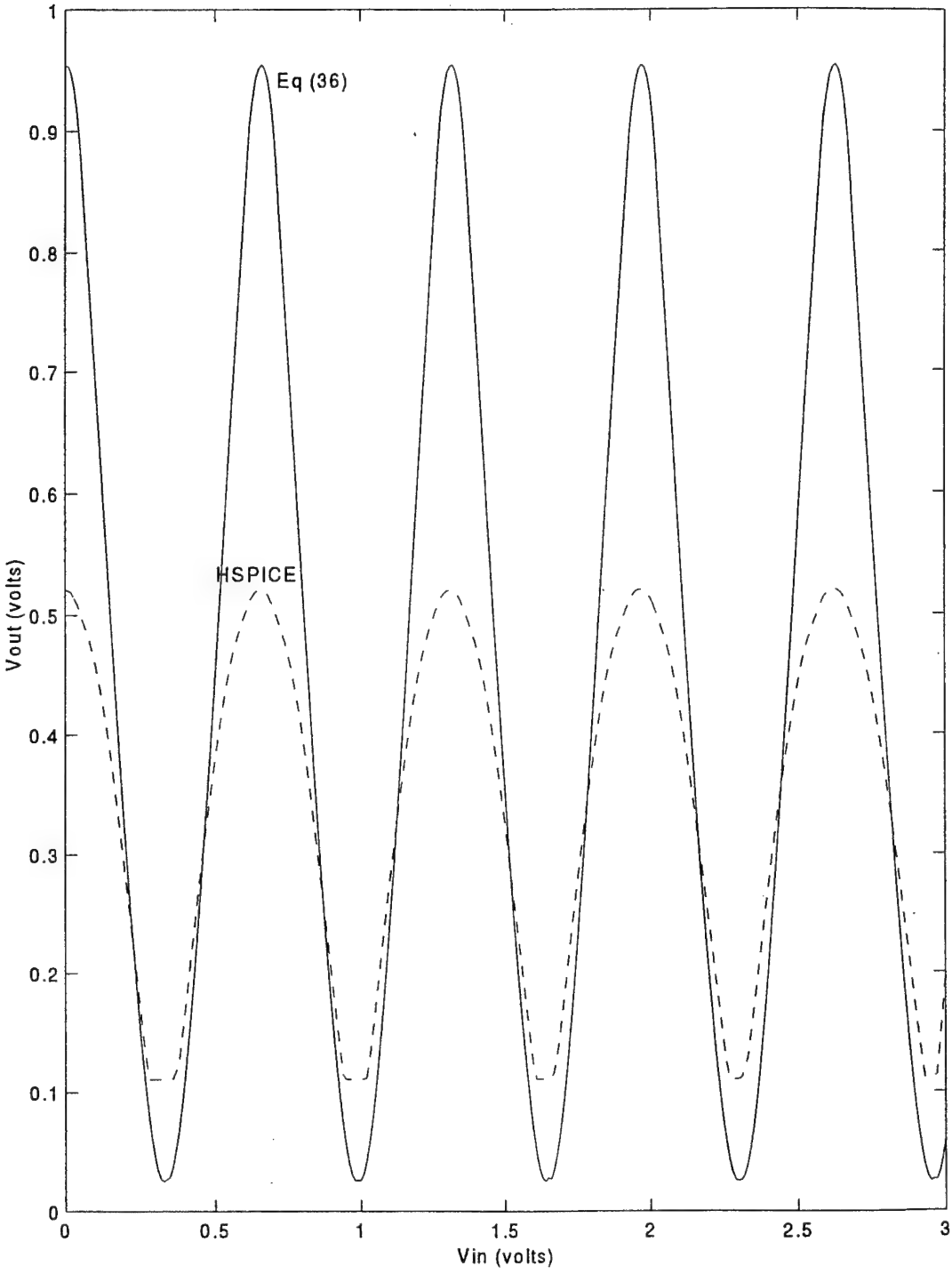

Figure 12: Initial HSPICE comparison of Mod 7 output voltage.

Table 5: Device Parameter Effects on Folded Output Waveform

Component	Parameter Changed	Effect on Folded Waveform
M5 and M6	Increase K_{56}	Decrease in peak-to-peak amplitude
M7 and M9	Increase K_7, K_9	Positive DC offset Increase in peak-to-peak amplitude
M1 and M2	Increase K_{12}	Increase in peak-to-peak amplitude
M3 and M4	Increase K_{34}	Decrease in folding period
I_1 and I_2	Increase current	Increase in peak-to-peak amplitude Increase in folding period
R_F	Increase resistance	Increase peak-to-peak amplitude

Figure 13. Based on the new K_{34} values for each modulus which are shown in Table 6, it is determined that the actual HSPICE transconductance values required for each stage, K_{34n}, can be approximated by

$$K_{34n} = 0.755K_{34} + \frac{(n-1)0.245K_{34}}{N_{fs}} \tag{50}$$

where n is the folding stage for which the transconductance is being determined, K_{34} is the initial value determined from the analysis, and N_{fs} is the number of folding stages within that modulus. The results of approximating the transconductance parameters using (50) are shown in Figure 14 by the dashed line, along with the actual values required in HSPICE which are represented by stars. The original value of K_{34} from the analysis is shown by the dotted line at the top of each plot.

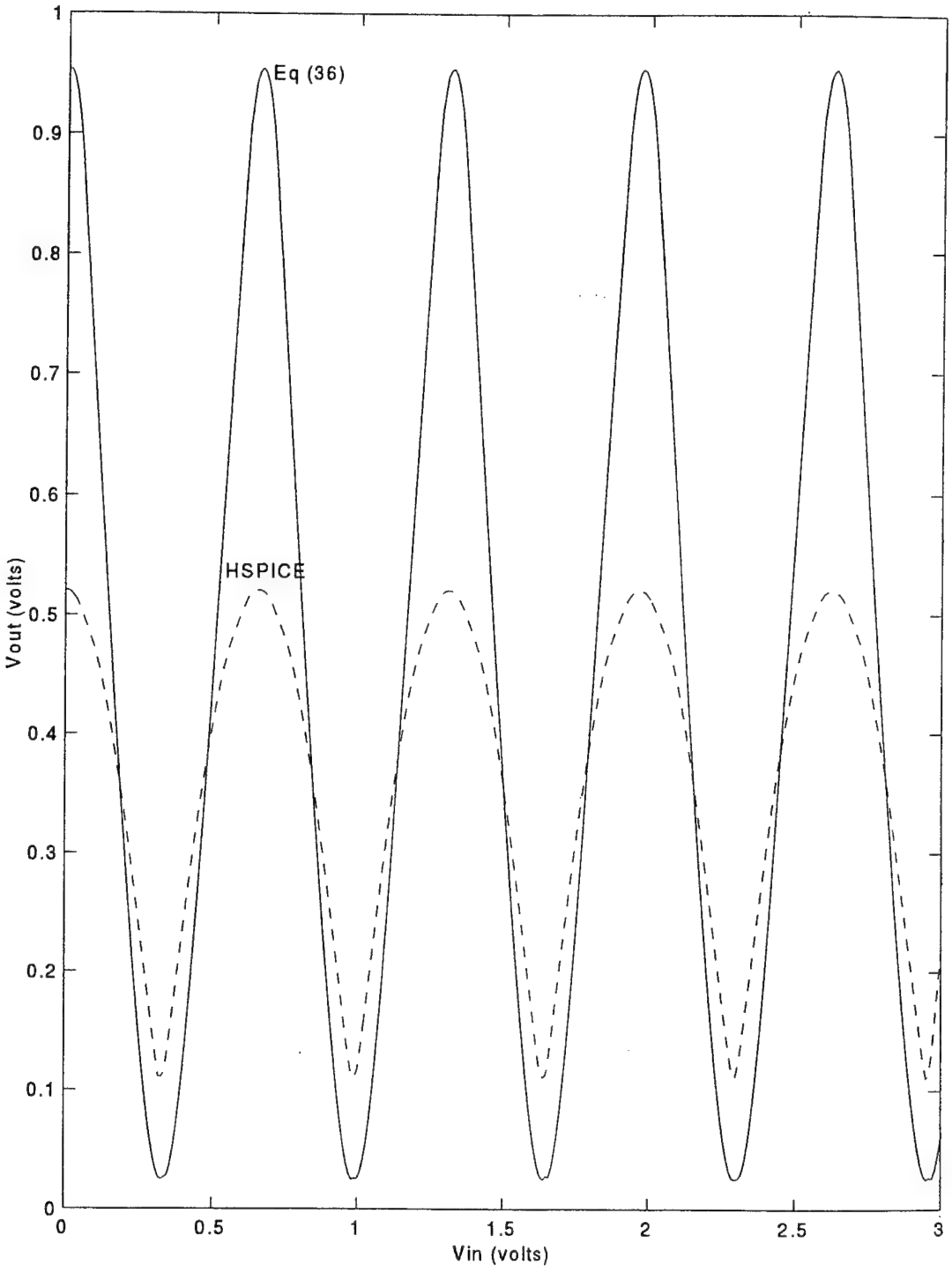

Figure 13: HSPICE comparison with fold widths corrected.

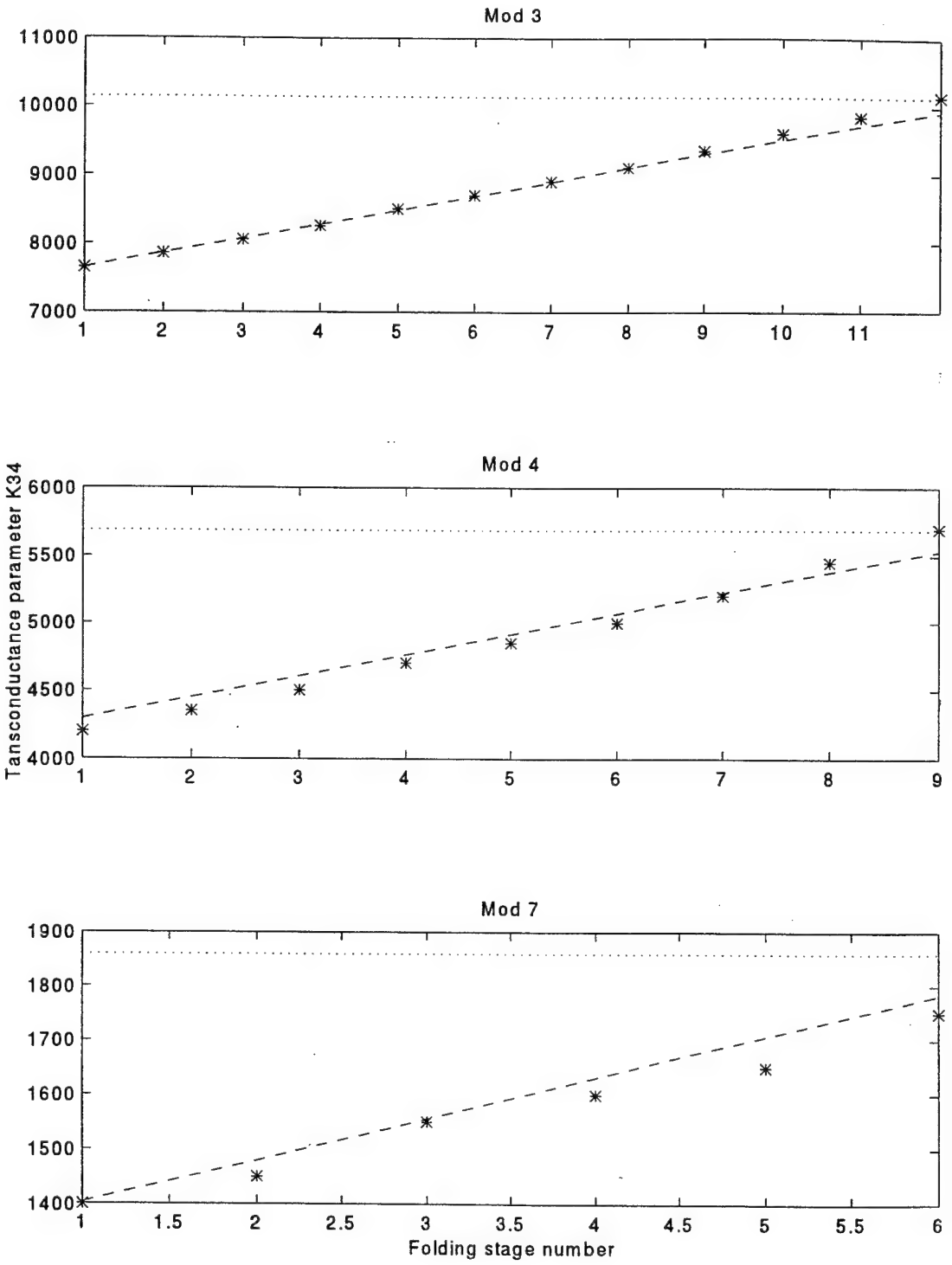

Figure 14: Results of approximation of HSPICE transconductance parameters for M3 and M4 (50).

Table 6: Revised Transconductance Parameter Values for HSPICE Simulation

Stage Number	**Mod 3** $K_{34}(\mu A/V^2)$	**Mod 4** $K_{34}(\mu A/V^2)$	**Mod 7** $K_{34}(\mu A/V^2)$
1	7650	4200	1400
2	7850	4350	1450
3	8050	4500	1550
4	8250	4700	1600
5	8500	4850	1650
6	8700	5000	1750
7	8900	5200	
8	9100	5450	
9	9350	5700	
10	9600		
11	9850		
12	10150		
Original Prediction	10131.6	5688.8	1859

Note: The predicted transconductance values for HSPICE are equal to twice the value of K determined in the analysis

Table 6 also illustrates that the transconductance parameters in HSPICE are twice as large as those used in the analysis. This is due to a difference in the way the two intrinsic transconductance parameters are defined. In the analysis, the intrinsic transconductance is defined by $K = \frac{1}{2}U_0 C_{ox}$ where U_0 is the majority carrier mobility constant and C_{ox} is the oxide capacitance. In HSPICE, the factor of one half is omitted. Both are multiplied by the ratio of the MOSFET gate width to length to obtain the effective transconductance parameter.

The other discrepancy observed in Figure 12 is the difference in the peak-to-peak amplitudes of the two waveforms. This is caused primarily by loading and feedback problems at the common input to the operational amplifier. While this is a major concern, the peak-to peak amplitude is easily corrected. From Table 5, it is seen that

by increasing either K_9 or R_F that the peak-to-peak amplitude can be increased to the desired value as shown in Figure 15.

While the design method presented does not produce exact correspondence with the HSPICE simulation results, it does provide a functional baseline circuit. Only minor modifications are required in order to achieve the desired folded output waveform in a more complex circuit analysis software product such as HSPICE. This provides a useful starting point when designing a folding circuit for new applications.

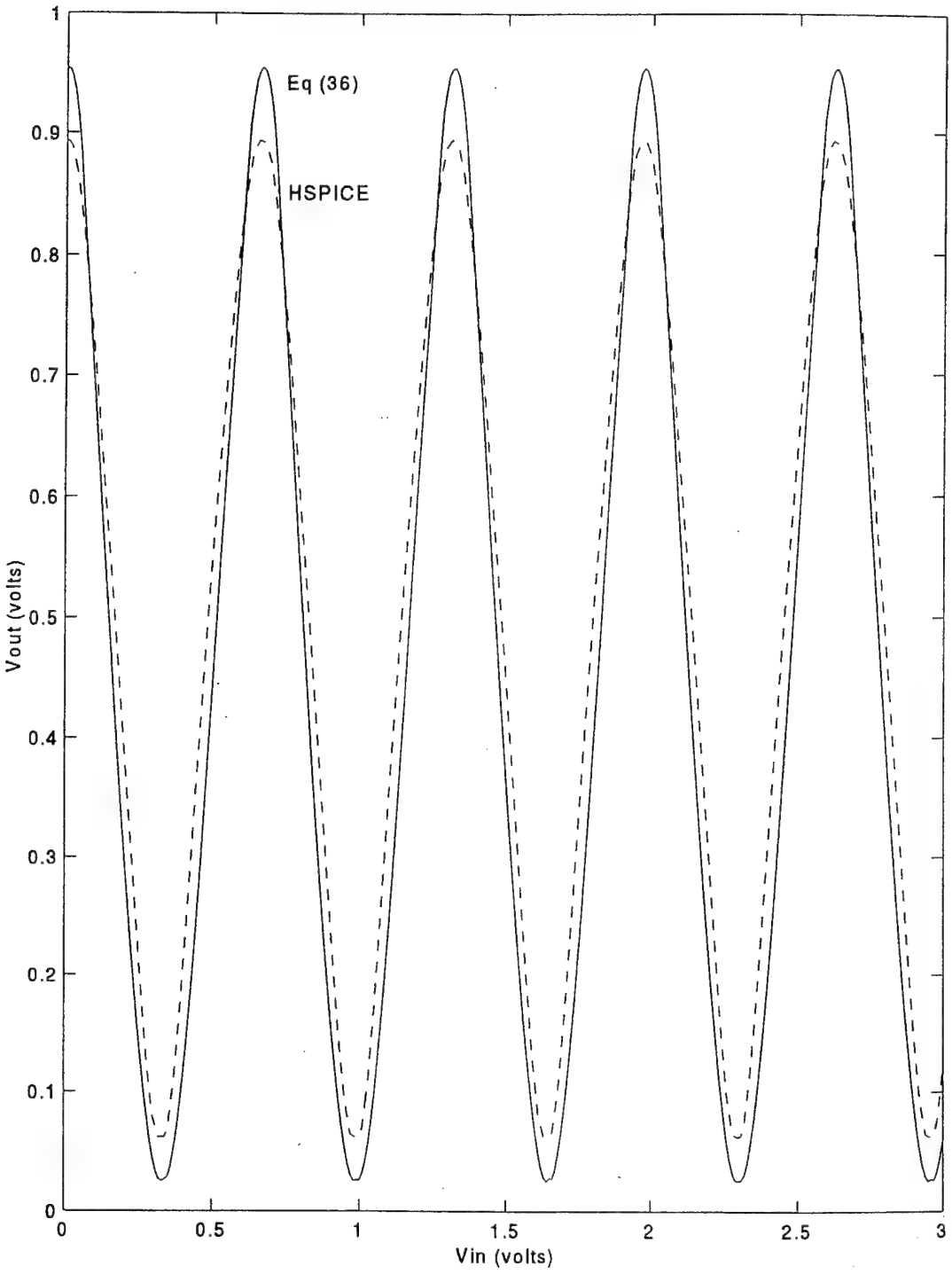

Figure 15: Final HSPICE output for Mod 7.

IV. DIGITAL CONVERSION

To verify that the analog preprocessor designed can effectively be incorporated in an ADC, the folded output waveforms of each channel are applied to the comparator circuits and PLAs which perform the analog-to digital conversion. The total number of comparators required for this system is

$$M = \sum_{i=1}^{N} m_i - 1 \tag{51}$$

which equals 11 for the system designed. The threshold voltages are selected for each channel to mid-level-quantize the input signal into the SNS format. This is accomplished by determining the value of the output waveform at each LSB. The LSB is determined from

$$LSB = \frac{V}{2^6} = \frac{V_{fwi}}{2m_i} \tag{52}$$

where V is the maximum input voltage and V_{fwi} is the fold width of modulus m_i. From (52) the LSB is determined to be 0.046875 volts. The comparator threshold voltages for each modulus are listed in Table 7. The comparator outputs (logical 1 or 0) are forwarded to the channel PLA which produces a binary representation of the number of active comparators, as shown in Figure 16. The SNS binary-coded outputs of each modulus are applied to the final PLA which determines the equivalent digital representation of the input signal.

Figure 17 shows the output of the ADC as a function of the input voltage. From this transfer function representation, numerous errors are evident. These errors are caused by encoding errors which occur at or near the transition code points. The encoding errors occur when some comparators change as they should but others do not. This results in a large encoding error. To resolve these discrepancies, a small decimation is included at each transition point [13]. This is accomplished using $2m$

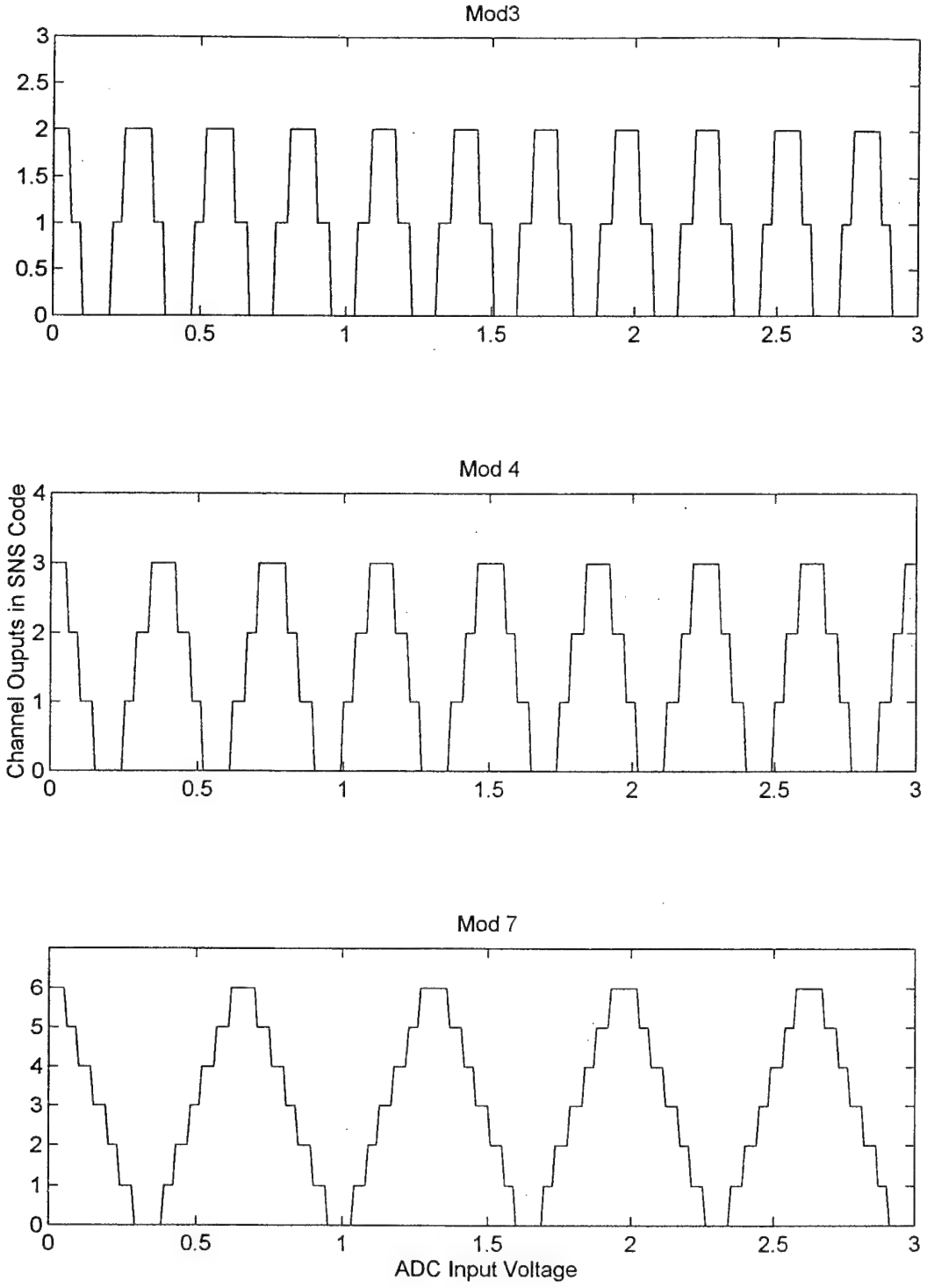

Figure 16: PLA outputs for each channel.

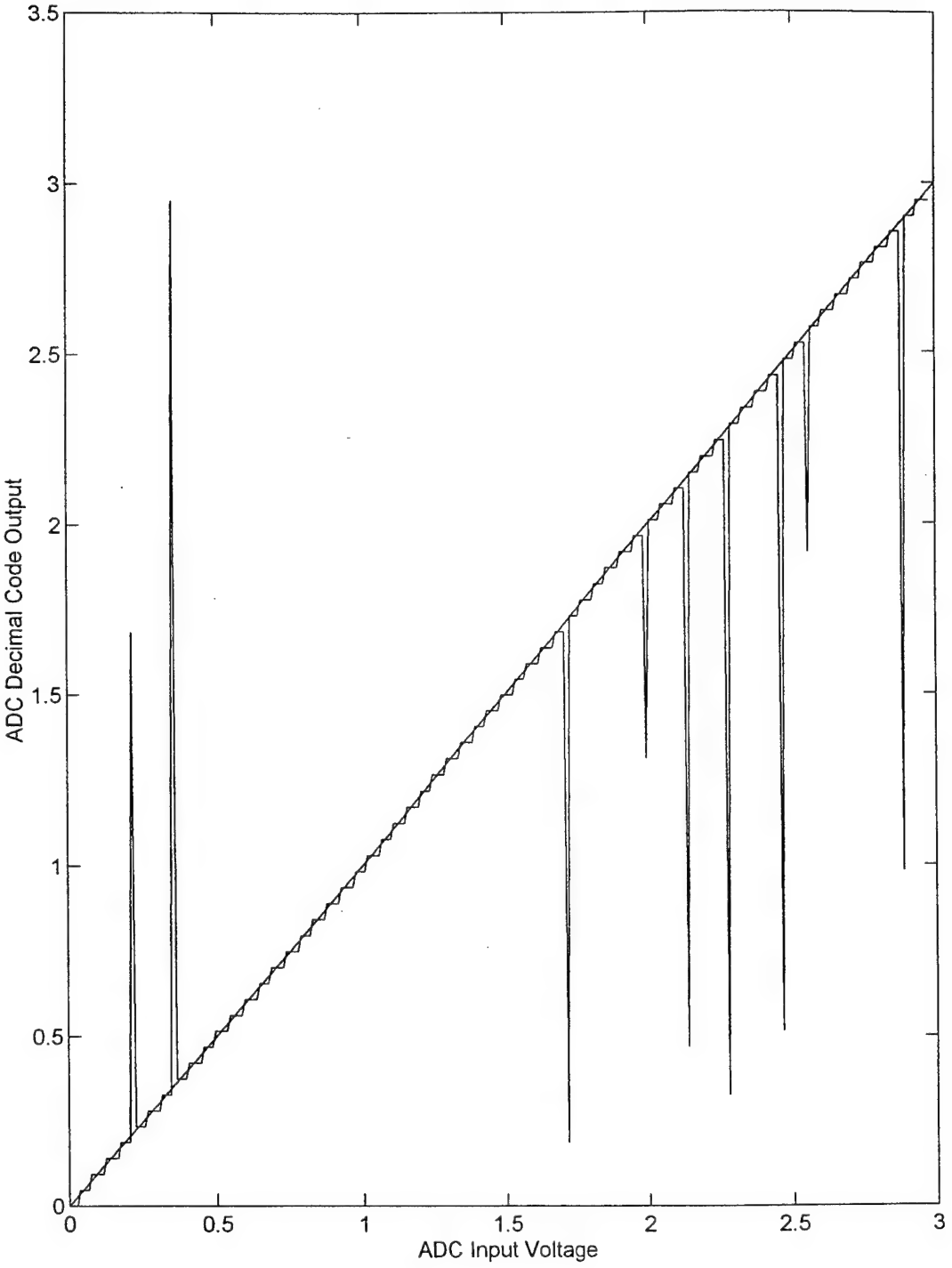

Figure 17: Steady-state transfer function for 6-bit SNS ADC without decimation.

vice $m-1$ comparators in the channel with the smallest modulus. This increases the number of comparators required for this 6-bit SNS ADC to 15 vice 11. A parity circuit is used to determine if the sample is within a decimation band. The parity circuit monitors the number of comparators which are turned on in the channel with the smallest modulus. If the input voltage is within one of the decimation bands, then the number of comparators turned on will be even, otherwise the number will be odd. If the input voltage falls within a decimation band, the potential for error exists and the sample is discarded. The output for this sample is then latched to its previous good sample. Comparator threshold voltages to implement a 10% LSB decimation band are listed in Table 8. The ADC transfer function response with 10% decimation, as shown in Figure 18, has eliminated the errors and produced a more accurate output. The dynamic operation of the decimation process results in a small known offset in the transfer function. The width of the offset is one-half the width of the decimation band.

Table 7: Comparator Threshold Voltages

Comparator Number	Threshold Voltage (V)		
	MOD 3	MOD 4	MOD 7
1	0.2570	0.1715	0.0760
2	0.6770	0.4526	0.2086
3	—	0.7854	0.3700
4	—	—	0.5500
5	—	—	0.7370
6	—	—	0.9100

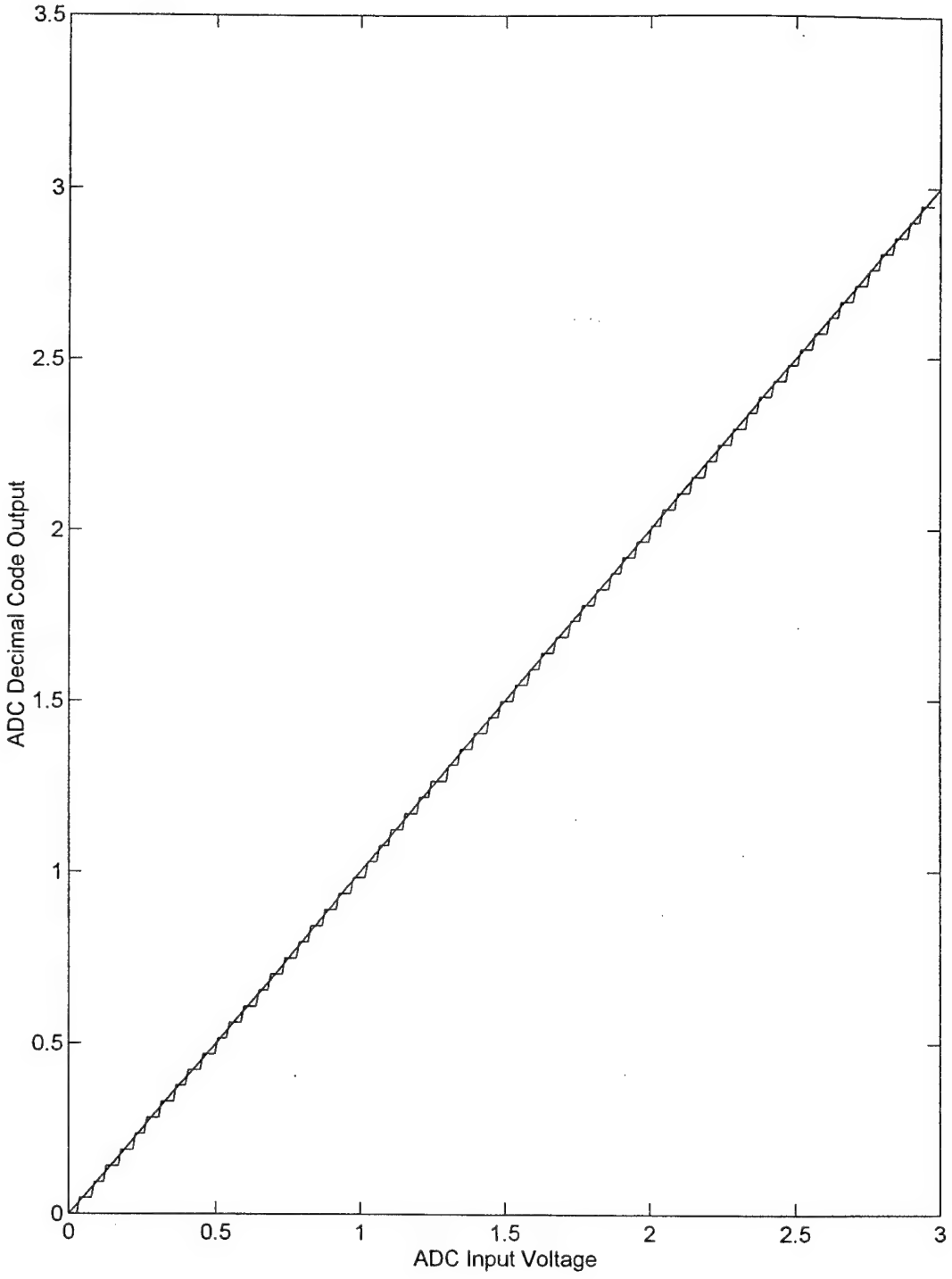

Figure 18: Steady-state transfer function for 6-bit SNS ADC with 10% LSB decimation.

Table 8: MOD 3 Comparator Threshold Voltages for 10% Decimation Band

Comparator Number	Threshold Voltage (V) MOD 3
1	0.0230
2	0.2390
3	0.2770
4	0.6517
5	0.7068
6	0.9659

V. EFFECTS OF FABRICATION TOLERANCES

With the design of the optimum SNS analog preprocessor complete, it is relevant to consider the effect of fabrication tolerances on the performance of the circuit. For such a preprocessor to be useful, it needs to be fabricated into an Application Specific Integrated Chip (ASIC) using Very Large Scale Integrated (VLSI) technology. The fabrication process, however, is subject to imperfections which cause certain MOSFET parameters to vary from the design specifications. Because fabrication tolerances differ from vendor to vendor and an ASIC is not being fabricated for the new preprocessor design at this time, this thesis will only consider the effect these fabrication tolerances have on circuit performance.

The principle parameters that are modified by the fabrication process are the intrinsic transconductance, K, and the threshold voltage, V_T, of the MOSFETs. For the purpose of illustrating the effect of fabrication tolerances on the 6-bit folding circuit, minimum and maximum values of K and V_T are chosen. Table 9 lists these values for both NFET and PFET transistors. These values are then incorporated into the analysis using a four-corner approach. By applying the four combinations of minimum and maximum MOSFET parameters for both the NFET and PFET, the circuit performance within these parameter limitations is observed.

Figure 19 shows the output voltage of the modulus 7 folding circuit for each of the four combinations of MOSFET parameters. The output voltage for the designed specifications is also shown for comparison. Curve A represents the output for maximum NFET values and maximum PFET values. Curve B represents the output for maximum NFET and minimum PFET values. Curve C shows the output for minimum NFET and maximum PFET values. Curve D is the output for minimum values of both NFET and PFET transistors. Curve E is the output of the circuit

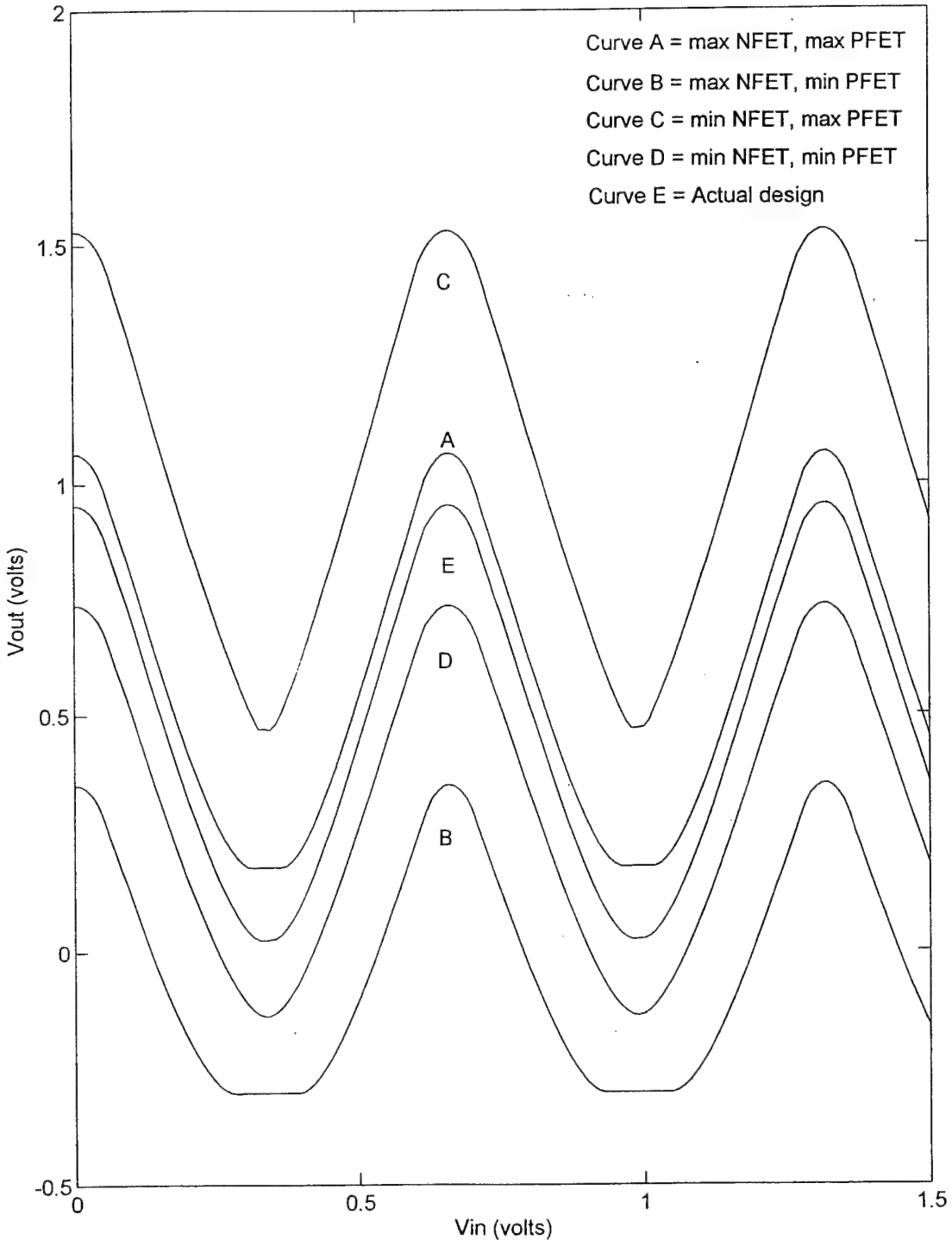

Figure 19: Effect on fabrication tolerances on Mod 7 output voltages using 4-corner analysis parameters.

Table 9: MOSFET Parameters for 4-Corner Analysis

NFET	MIN $K(\mu A/V^2)$	$V_T(V)$	MAX $K(\mu A/V^2)$	$V_T(V)$
M_1, M_2	810	1.65	990	1.75
M_3, M_4	Mod 3: 4559 Mod 4: 2560 Mod 7: 8369	1.30	Mod 3: 5572 Mod 4: 3129 Mod 7: 1022	1.50
M_8	90	0.65	110	0.85
M_9	9	1.45	11	1.65
M_{11}	90	0.65	110	0.85
PFET	**MIN** $K(\mu A/V^2)$	$V_T(V)$	**MAX** $K(\mu A/V^2)$	$V_T(V)$
M_5, M_6	18	−0.85	22	−0.65
M_7	720	−0.85	880	−0.65
M_{10}	81	−0.85	99	−0.65

as originally designed. From Figure 19 it is shown that the output voltage waveform is very sensitive to the parameter changes caused by fabrication tolerances. Effects include a change in the peak-to-peak voltage, DC offset, and distortion (flattening) at the bottoms of some waveforms. The waveforms still retain, however, the proper folding period and shape for SNS preprocessing.

As long as the folded waveform retains its required folding period and is not distorted , the comparator threshold values can be adjusted to properly mid-level quantize the signal and achieve the desired output. The primary cause of waveform distortion occurs when V_3 is pushed below the threshold voltage of M9. This effectively turns M9 off and accounts for the flattening of the lower portion of the distorted waveforms (Curves A and Curve B). In order to accommodate fabrication tolerances,

the ratio of K_7 to K_8 can be altered so that for the worst case (Curve B), V_3 remains above the threshold voltage for M9. If this does not create a distortion in the upper curve (Curve C), the circuit will be able to accommodate the effects of fabrication tolerances and still be incorporated into an ADC. The comparator circuits will, however, have to be adjusted to fit the waveform produced.

VI. CONCLUDING REMARKS

A thorough numerical analysis of a CMOS analog folding circuit architecture has been presented. This analysis has been incorporated into a detailed circuit design process which provides an approach which can be used to implement a folding circuit into an analog preprocessing architecture. A preprocessor for a 6-bit SNS ADC has been designed using this process and has been simulated in HSPICE. A relationship has been derived which estimates the required transconductance parameters for M3 and M4 for each folding stage. By incorporating this relationship, the design serves as an excellent baseline model which produces a functional folded output in HSPICE simulations. Applicability of this preprocessor is proven by completing the conversion process and observing its transfer function results. Decimation bands are included in the ADC to remove coding errors.

A four-corners approach has been presented to investigate the effect of fabrication tolerances on circuit performance. Minor fabrication tolerances are shown to cause peak-to-peak voltage variations, DC offsets, and distortion in the output waveforms. The folding periods and general shape of the waveforms remain intact. Therefore, the output, if not distorted, is still viable in SNS ADC applications although the comparator thresholds would have to reset once the final output waveform is determined. Modifications to the folding circuit design parameters are recommended to account for these tolerances.

The frequency response of CMOS folding circuits is unsuitable for most high frequency applications. This is due, in part, to the nature of folding circuits because they increase the apparent frequency of the input signal by a factor equal to the number of times the signal is folded. Additionally, CMOS transistors are not well suited for very high frequency applications because of the large inherent gate capacitance

and low transconductance relative to bi-polar junction transistors. Further research in high frequency folding circuits should be devoted to gallium arsenide devices, which have excellent performance characteristics in high speed applications.

APPENDIX A. MATLAB FILE

```
%MATLAB-m file used to perform analysis of the 6 bit CMOS
%folding circuit architecture devoloped in this thesis.
%This particular file produces the Modulus 7 output
%voltage. Reference voltages, number of folding stages, and
%K3 and K4 can be changed to produce outputs of Moduli 3
%and 4.

%%%% Circuit Initialization %%%%

% Input Voltage
Vin=(-1:.01:3);
x=401;          %number of input samples (used for indexing)

% Reference voltages for each folding stage
  %(folding width times folding stage number)
Vref=.656*[0,1,2,3,4,5];

%Power Supplies
Vdd=5;
Vss=-5;

%MOSFET threshold voltages in volts
 %Zero Bias Threshold voltages for NFET and PFET
Vtn=.75;
Vtp=-.75;
 %Threshlod Voltages for MOSFETs affected by
  % channel length modulation
Vt1=1.75;
Vt2=1.75;
Vt3=1.4;
Vt4=1.4;
Vt9=1.55;

%Current source value in microamps
I1=100;
I2=100;

%MOSFET transconductances in microamps/volt^2
K1=900; K2=900; K3=929.5; K4=929.5;
K5=20; K6=20; K7=800; K8=100; K9=10;
K10=90; K11=100;
%Chanel length modulation parameters
l7=-1/10;
l8=1/15;
l10=-1/10;
l11=1/15;
```

```
%Feedback resistance and R1 in Kohms
Rf=20;
R1=1;

%Vector initialization for storing outputs
Vsumop=zeros(1,x+1);
Vout=zeros(1,x+1);

%%%% Bias point analysis of VGS %%%%

%Lower differential pair
VGS3=Vt3+sqrt(I2/(2*K3));          % Eq  2
%Upper differentail pair
VGS1=Vt1+sqrt(I1/(2*K1));          % Eq  4

%%%% Differential Input Analysis %%%%

%Lower Differential Pair M3, M4
for z=1:6                          %for each folding stage
V3=1.55*ones(1,x+1);               %intialize V3
for j=1:x                           %run through the range of
                                     %input voltages
Vid3(j)=Vin(j)-Vref(z);            % Diff input voltage
%Calculation of diff current
if abs(Vid3(j)) <= (sqrt(2)*(VGS3-Vtn))
   id34(j)=(I2/(VGS3-Vtn))*(Vid3(j)/2)*sqrt(1-(Vid3(j)
           /(2*(VGS3-Vtn)))^2);
   elseif  Vid3(j) >= sqrt(2)*(VGS3-Vtn)
      id34(j)=I2/2;
   else
      id34(j)=-I2/2;
   end

%Determine i3 and i4
i3(j)=I2/2+id34(j);                    % from Eq 12
i4(j)=I2/2-id34(j);                    % from Eq 13


%Calculation of inputs voltages to upper diff amp
V1(j)=Vdd+Vtp-sqrt(i3(j)/(K5));
V2(j)=Vdd+Vtp-sqrt(i4(j)/(K6));

%Upper DifferentialPair

% Differntial Voltage
Vid1(j)=V1(j)-V2(j);

% Determine differential current
```

```
  if abs(Vid1(j)) <= (sqrt(2)*(VGS1-Vt1))
     id12(j)=(I1/(VGS1-Vt1))*(Vid1(j)/2)*sqrt(1-(Vid1(j)
              /(2*(VGS1-Vt1)))^2);
  elseif  Vid1(j) >= sqrt(2)*(VGS1-Vt1)
     id12(j)=I1/2;
  else
     id12(j)=-I1/2;
   end
%deterine drain currents i1 and i2
i1(j)=I1/2+id12(j);                          % from Eq 19
i2(j)=I1/2-id12(j);                          % from Eq 20

%determine source voltages of M1 and M2
Vs1(j)=V1(j)-Vt1-sqrt(i1(j)/(K1));           % from Eq 21
Vs2(j)=V2(j)-Vt2-sqrt(i2(j)/(K2));           % from Eq 22

% Folded output from upper diffamp
Vf(j)=max(Vs1(j),Vs2(j));                    % from Eq 23

% Output of channel voltage shifting arrangement M7,M8
% without channel length modulation
%V3(j)=sqrt(K7/K8)*(Vdd+Vtp-Vo(j))+Vss+Vtn; % from Eq 25

% with channel length modulation, from Eq 29
V3(j+1)=sqrt((K7/K8)*(Vf(j)-Vdd-Vtp)^2*(1+l7*(V3(j)-Vdd))
        /(1+l8*(V3(j)-Vss)))+Vss+Vtn;

% Source voltage of M9, Vs9, from Eq 32
Vs9(j) = (V3(j)-Vt9)+(1000/(2*K9*R1))-(1/2)*sqrt
((2*(V3(j)-Vt9)+(1000/(K9*R1)))^2-4*(V3(j)-Vt9)^2));

%%%% Output Stage of Folding Circuit  %%%%
% Input to opamp equals combination of  all folding stages
Vsumop(j)=Vsumop(j)+Vs9(j);

% Output of summing opamp, V4
V4(j)=-Rf*Vsumop(j);                    %from Eq 33

% Final Output  Voltage, Vout
% without channel length modulation, from Eq 35
%Vout7(j)=sqrt(K10/(K11))*(Vdd+Vtp-Vop7(j))+Vss+Vtn;

% with channel length modulaton, from Eq 36
Vout7(j+1)=sqrt((K10/(K11))*(Vop7(j)-Vdd-Vtp)^2*
(1+l10*(Vout7(j)-Vdd))/(1+l11*(Vout7(j)-Vss)))+Vss+Vtn;
end
end
```

APPENDIX B. HSPICE FILES

A. MODULUS 3 FOLDING CIRCUIT

```
** mod3f12.sp
** This file implements a mod 3 12 stage folding circuit
** Technology: scmos

* Model statements for mosfets
.MODEL nnf NMOS(LEVEL=2 VTO=+0.75 TOX=400E-10
+ NSUB=8.0E+15 XJ=0.15U LD=0.20U U0=650 UCRIT=0.62E5
+ UEXP=0.125 VMAX=5.1E4 NEFF=4.0 DELTA=1.4 RSH=36
+ CGSO=1.95E-10 CGDO=1.95E-10 CJ=195U CJSW=500P MJ=0.76
+ MJSW=0.30 PB=0.8 PHI=0.6 GAMMA=0.5 LAMBDA=0.0667
+ KP=10.0e-5)

.MODEL npf PMOS(LEVEL=2 VTO=-0.75 TOX=400E-10
+ NSUB=6.0E+15 XJ=0.05U LD=0.20U U0=255 UCRIT=0.86E5
+ UEXP=0.29 VMAX=3.0E4 NEFF=2.65 DELTA=1.0 RSH=101
+ CGSO=1.9E-10 CGDO=1.9E-10 CJ=250U CJSW=350P MJ=0.535
+ MJSW=0.34 PB=0.8 PHI=0.6 GAMMA=0.5 LAMBDA=-0.1
+ KP=4.0e-5)

*Sources
Vdd  1   0  5V
Vss  115 0 -5V
Vop+ 128 0  5V
Vop- 124 0 -5V

*Input signal
Vin 103 0 PWL 0 0.0V, 0.1s 3.0V

** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 103 = Vin
** NODE: 115 = Vss
** NODE: 124 = Vop-
** NODE: 128 = Vop+
** NODE: 130 = Vout

* Reference voltages for folds
* Vref1 = 0.0v
Vref2 205 0 0.281V
Vref3 305 0 0.562V
Vref4 405 0 0.843
Vref5 505 0 1.124
Vref6 605 0 1.405
Vref7 705 0 1.686
```

```
Vref8 805 0 1.967
Vref9 905 0 2.248
Vref10 1005 0 2.529
Vref11 1105 0 2.81
Vref12 1205 0 3.091

*Current sources
I11 112 115 .1ma
I21 100 115 .1ma
I12 212 115 .1ma
I22 200 115 .1ma
I13 312 115 .1ma
I23 300 115 .1ma
I14 412 115 .1ma
I24 400 115 .1ma
I15 512 115 .1ma
I25 500 115 .1ma
I16 612 115 .1ma
I26 600 115 .1ma
I17 712 115 .1ma
I27 700 115 .1ma
I18 812 115 .1ma
I28 800 115 .1ma
I19 912 115 .1ma
I29 900 115 .1ma
I110 1012 115 .1ma
I210 1000 115 .1ma
I111 1112 115 .1ma
I211 1100 115 .1ma
I112 1212 115 .1ma
I212 1200 115 .1ma

* Input resistors for summing amplifier
R1 113 127 1K
R2 213 127 1K
R3 313 127 1K
R4 413 127 1K
R5 513 127 1K
R6 613 127 1K
R7 713 127 1K
R8 813 127 1K
R9 913 127 1K
R10 1013 127 1K
R11 1113 127 1K
R12 1213 127 1K
```

```
** Folding stages

* Stage 1
M11A 1 102 112 115 nnf L=2.0U W=36.0U
M12A 1 101 112 115 nnf L=2.0U W=36.0U
M13  102 103 100 115 nnf L=2.0U W=153.0U
M14  100 0 101 115 nnf L=2.0U W=153.0U
M15  102 102 1 1 npf L=2.0U W=2.0U
M16  1 101 101 1 npf L=2.0U W=2.0U
M17A 1 112 114 1 npf L=2.0U W=80.0U
M18  115 114 114 115 nnf L=2.0U W=4.0U
M19  113 114 1 115 nnf L=10.0U W=2.0U

* Stage 2
M21A 1 202 212 115 nnf L=2.0U W=36.0U
M22A 1 201 212 115 nnf L=2.0U W=36.0U
M23  202 103 200 115 nnf L=2.0U W=157.0U
M24  200 205 201 115 nnf L=2.0U W=157.0U
M25  202 202 1 1 npf L=2.0U W=2.0U
M26  1 201 201 1 npf L=2.0U W=2.0U
M27A 1 212 214 1 npf L=2.0U W=80.0U
M28  115 214 214 115 nnf L=2.0U W=4.0U
M29  213 214 1 115 nnf L=10.0U W=2.0U

* Stage 3
M31A 1 302 312 115 nnf L=2.0U W=36.0U
M32A 1 301 312 115 nnf L=2.0U W=36.0U
M33  302 103 300 115 nnf L=2.0U W=161.0U
M34  300 305 301 115 nnf L=2.0U W=161.0U
M35  302 302 1 1 npf L=2.0U W=2.0U
M36  1 301 301 1 npf L=2.0U W=2.0U
M37A 1 312 314 1 npf L=2.0U W=80.0U
M38  115 314 314 115 nnf L=2.0U W=4.0U
M39  313 314 1 115 nnf L=10.0U W=2.0U


* Stage 4
M41A 1 402 412 115 nnf L=2.0U W=36.0U
M42A 1 401 412 115 nnf L=2.0U W=36.0U
M43  402 103 400 115 nnf L=2.0U W=165.0U
M44  400 405 401 115 nnf L=2.0U W=165.0U
M45  402 402 1 1 npf L=2.0U W=2.0U
M46  1 401 401 1 npf L=2.0U W=2.0U
M47A 1 412 414 1 npf L=2.0U W=80.0U
M48  115 414 414 115 nnf L=2.0U W=4.0U
M49  413 414 1 115 nnf L=10.0U W=2.0U
```

```
* Stage 5
M51A 1 502 512 115 nnf L=2.0U W=36.0U
M52A 1 501 512 115 nnf L=2.0U W=36.0U
M53  502 103 500 115 nnf L=2.0U W=170.0U
M54  500 505 501 115 nnf L=2.0U W=170.0U
M55  502 502 1 1 npf L=2.0U W=2.0U
M56  1 501 501 1 npf L=2.0U W=2.0U
M57A 1 512 514 1 npf L=2.0U W=80.0U
M58  115 514 514 115 nnf L=2.0U W=4.0U
M59  513 514 1 115 nnf L=10.0U W=2.0U

* Stage 6
M61A 1 602 612 115 nnf L=2.0U W=36.0U
M62A 1 601 612 115 nnf L=2.0U W=36.0U
M63  602 103 600 115 nnf L=2.0U W=174.0U
M64  600 605 601 115 nnf L=2.0U W=174.0U
M65  602 602 1 1 npf L=2.0U W=2.0U
M66  1 601 601 1 npf L=2.0U W=2.0U
M67A 1 612 614 1 npf L=2.0U W=80.0U
M68  115 614 614 115 nnf L=2.0U W=4.0U
M69  613 614 1 115 nnf L=10.0U W=2.0U

* Stage 7
M71A 1 702 712 115 nnf L=2.0U W=36.0U
M72A 1 701 712 115 nnf L=2.0U W=36.0U
M73  702 103 700 115 nnf L=2.0U W=178.0U
M74  700 705 701 115 nnf L=2.0U W=178.0U
M75  702 702 1 1 npf L=2.0U W=2.0U
M76  1 701 701 1 npf L=2.0U W=2.0U
M77A 1 712 714 1 npf L=2.0U W=80.0U
M78  115 714 714 115 nnf L=2.0U W=4.0U
M79  713 714 1 115 nnf L=10.0U W=2.0U

* Stage 8
M81A 1 802 812 115 nnf L=2.0U W=36.0U
M82A 1 801 812 115 nnf L=2.0U W=36.0U
M83  802 103 800 115 nnf L=2.0U W=182.0U
M84  800 805 801 115 nnf L=2.0U W=182.0U
M85  802 802 1 1 npf L=2.0U W=2.0U
M86  1 801 801 1 npf L=2.0U W=2.0U
M87A 1 812 814 1 npf L=2.0U W=80.0U
M88  115 814 814 115 nnf L=2.0U W=4.0U
M89  813 814 1 115 nnf L=10.0U W=2.0U

* Stage 9
M91A 1 902 912 115 nnf L=2.0U W=36.0U
M92A 1 901 912 115 nnf L=2.0U W=36.0U
M93  902 103 900 115 nnf L=2.0U W=187.0U
```

```
M94   900 905 901 115 nnf L=2.0U W=187.0U
M95   902 902 1 1 npf L=2.0U W=2.0U
M96   1 901 901 1 npf L=2.0U W=2.0U
M97A  1 912 914 1 npf L=2.0U W=80.0U
M98   115 914 914 115 nnf L=2.0U W=4.0U
M99   913 914 1 115 nnf L=10.0U W=2.0U

* Stage 10
M101A 1 1002 1012 115 nnf L=2.0U W=36.0U
M102A 1 1001 1012 115 nnf L=2.0U W=36.0U
M103  1002 103 1000 115 nnf L=2.0U W=192.0U
M104  1000 1005 1001 115 nnf L=2.0U W=192.0U
M105  1002 1002 1 1 npf L=2.0U W=2.0U
M106  1 1001 1001 1 npf L=2.0U W=2.0U
M107A 1 1012 1014 1 npf L=2.0U W=80.0U
M108  115 1014 1014 115 nnf L=2.0U W=4.0U
M109  1013 1014 1 115 nnf L=10.0U W=2.0U

* Stage 11
M111A 1 1102 1112 115 nnf L=2.0U W=36.0U
M112A 1 1101 1112 115 nnf L=2.0U W=36.0U
M113  1102 103 1100 115 nnf L=2.0U W=197.0U
M114  1100 1105 1101 115 nnf L=2.0U W=197.0U
M115  1102 1102 1 1 npf L=2.0U W=2.0U
M116  1 1101 1101 1 npf L=2.0U W=2.0U
M117A 1 1112 1114 1 npf L=2.0U W=80.0U
M118  115 1114 1114 115 nnf L=2.0U W=4.0U
M119  1113 1114 1 115 nnf L=10.0U W=2.0U

* Stage 12
M121A 1 1202 1212 115 nnf L=2.0U W=36.0U
M122A 1 1201 1212 115 nnf L=2.0U W=36.0U
M123  1202 103 1200 115 nnf L=2.0U W=203.0U
M124  1200 1205 1201 115 nnf L=2.0U W=203.0U
M125  1202 1202 1 1 npf L=2.0U W=2.0U
M126  1 1201 1201 1 npf L=2.0U W=2.0U
M127A 1 1212 1214 1 npf L=2.0U W=80.0U
M128  115 1214 1214 115 nnf L=2.0U W=4.0U
M129  1213 1214 1 115 nnf L=10.0U W=2.0U

* OP Amp circuit
M1001 126 127 122 115 nnf L=10.0U W=40.0U
M1002 122 0 125 115 nnf L=10.0U W=40.0U
M1003 126 126 128 1 npf L=22.0U W=10.0U
M1004 128 126 125 1 npf L=22.0U W=10.0U
M1005 129 125 128 1 npf L=10.0U W=45.0U
M1006 124 123 129 115 nnf L=10.0U W=10.0U
M1007 122 123 124 115 nnf L=50.0U W=10.0U
```

```
M1008 124 123 123 115 nnf L=10.0U W=10.0U

*Op amp Resistors and capacitor
Rbias 128 123 2K
Rf  127 129 20K
Rz  125 999 13K
Cc 999 129 5pF

* Final voltage shifter
M1009 128 129 130 1 npf L=2.0U W=10.0U
M1010 124 130 130 115 nnf L=2.0U W=4.0U

****Simulation Parameters********
.tran 333333ns .1s
.PRINT V(130)
.option dcon=1 post probe
* .tran 100000ns .1s
.end
```

B. MOD 4 FOLDING CIRCUIT

```
** mod4f9.sp
** This file implements a mod 4, 9 stage folding corcuit
** Technology: scmos
* Model statements for mosfets

.MODEL nnf NMOS(LEVEL=2 VTO=+0.75 TOX=400E-10
+ NSUB=8.0E+15 XJ=0.15U LD=0.20U U0=650 UCRIT=0.62E5
+ UEXP=0.125 VMAX=5.1E4 NEFF=4.0 DELTA=1.4 RSH=36
+ CGSO=1.95E-10 CGDO=1.95E-10 CJ=195U CJSW=500P MJ=0.76
+ MJSW=0.30 PB=0.8 PHI=0.6 GAMMA=0.5 LAMBDA=0.0667
+ KP=10.0e-5)

.MODEL npf PMOS(LEVEL=2 VTO=-0.75 TOX=400E-10
+ NSUB=6.0E+15 XJ=0.05U LD=0.20U U0=255 UCRIT=0.86E5
+ UEXP=0.29 VMAX=3.0E4 NEFF=2.65 DELTA=1.0 RSH=101
+ CGSO=1.9E-10 CGDO=1.9E-10 CJ=250U CJSW=350P MJ=0.535
+ MJSW=0.34 PB=0.8 PHI=0.6 GAMMA=0.5 LAMBDA=-0.1
+ KP=4.0e-5)


** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 103 = Vin
** NODE: 115 = Vss
** NODE: 130 = Vout
```

```
*Input signal
Vin 103 0 PWL 0 0.0V, 0.1s 3.0V
*Sources
Vdd  1   0  5V
Vss  115 0 -5V
Vop+ 128 0  5V
Vop- 124 0 -5V

* Reference voltages for folds
* Vref1 = 0.0v
Vref2 205 0 0.375
Vref3 305 0 0.75
Vref4 405 0 1.125
Vref5 505 0 1.5
Vref6 605 0 1.875
Vref7 705 0 2.25
Vref8 805 0 2.625
Vref9 905 0 3

*Current sources
I11 112 115 .1ma
I21 100 115 .1ma
I12 212 115 .1ma
I22 200 115 .1ma
I13 312 115 .1ma
I23 300 115 .1ma
I14 412 115 .1ma
I24 400 115 .1ma
I15 512 115 .1ma
I25 500 115 .1ma
I16 612 115 .1ma
I26 600 115 .1ma
I17 712 115 .1ma
I27 700 115 .1ma
I18 812 115 .1ma
I28 800 115 .1ma
I19 912 115 .1ma
I29 900 115 .1ma

* Input resistors for summing amplifier
R1 113 127 1K
R2 213 127 1K
R3 313 127 1K
R4 413 127 1K
R5 513 127 1K
R6 613 127 1K
R7 713 127 1K
```

```
R8 813 127 1K
R9 913 127 1K

** Folding stages
* Stage 1
M11A 1 102 112 115 nnf L=2.0U W=36.0U
M12A 1 101 112 115 nnf L=2.0U W=36.0U
M13  102 103 100 115 nnf L=2.0U W=84.0U
M14  100 0 101 115 nnf L=2.0U W=84.0U
M15  102 102 1 1 npf L=2.0U W=2.0U
M16  1 101 101 1 npf L=2.0U W=2.0U
M17A 1 112 114 1 npf L=2.0U W=80.0U
M18  115 114 114 115 nnf L=2.0U W=4.0U
M19  113 114 1 115 nnf L=10.0U W=2.0U

* Stage 2
M21A 1 202 212 115 nnf L=2.0U W=36.0U
M22A 1 201 212 115 nnf L=2.0U W=36.0U
M23  202 103 200 115 nnf L=2.0U W=87.0U
M24  200 205 201 115 nnf L=2.0U W=87.0U
M25  202 202 1 1 npf L=2.0U W=2.0U
M26  1 201 201 1 npf L=2.0U W=2.0U
M27A 1 212 214 1 npf L=2.0U W=80.0U
M28  115 214 214 115 nnf L=2.0U W=4.0U
M29  213 214 1 115 nnf L=10.0U W=2.0U

* Stage 3
M31A 1 302 312 115 nnf L=2.0U W=36.0U
M32A 1 301 312 115 nnf L=2.0U W=36.0U
M33  302 103 300 115 nnf L=2.0U W=90.0U
M34  300 305 301 115 nnf L=2.0U W=90.0U
M35  302 302 1 1 npf L=2.0U W=2.0U
M36  1 301 301 1 npf L=2.0U W=2.0U
M37A 1 312 314 1 npf L=2.0U W=80.0U
M38  115 314 314 115 nnf L=2.0U W=4.0U
M39  313 314 1 115 nnf L=10.0U W=2.0U

* Stage 4
M41A 1 402 412 115 nnf L=2.0U W=36.0U
M42A 1 401 412 115 nnf L=2.0U W=36.0U
M43  402 103 400 115 nnf L=2.0U W=94.0U
M44  400 405 401 115 nnf L=2.0U W=94.0U
M45  402 402 1 1 npf L=2.0U W=2.0U
M46  1 401 401 1 npf L=2.0U W=2.0U
M47A 1 412 414 1 npf L=2.0U W=80.0U
M48  115 414 414 115 nnf L=2.0U W=4.0U
M49  413 414 1 115 nnf L=10.0U W=2.0U
```

```
* Stage 5
M51A 1 502 512 115 nnf L=2.0U W=36.0U
M52A 1 501 512 115 nnf L=2.0U W=36.0U
M53  502 103 500 115 nnf L=2.0U W=97.0U
M54  500 505 501 115 nnf L=2.0U W=97.0U
M55  502 502 1 1 npf L=2.0U W=2.0U
M56  1 501 501 1 npf L=2.0U W=2.0U
M57A 1 512 514 1 npf L=2.0U W=80.0U
M58  115 514 514 115 nnf L=2.0U W=4.0U
M59  513 514 1 115 nnf L=10.0U W=2.0U

* Stage 6
M61A 1 602 612 115 nnf L=2.0U W=36.0U
M62A 1 601 612 115 nnf L=2.0U W=36.0U
M63  602 103 600 115 nnf L=2.0U W=100.0U
M64  600 605 601 115 nnf L=2.0U W=100.0U
M65  602 602 1 1 npf L=2.0U W=2.0U
M66  1 601 601 1 npf L=2.0U W=2.0U
M67A 1 612 614 1 npf L=2.0U W=80.0U
M68  115 614 614 115 nnf L=2.0U W=4.0U
M69  613 614 1 115 nnf L=10.0U W=2.0U

* Stage 7
M71A 1 702 712 115 nnf L=2.0U W=36.0U
M72A 1 701 712 115 nnf L=2.0U W=36.0U
M73  702 103 700 115 nnf L=2.0U W=104.0U
M74  700 705 701 115 nnf L=2.0U W=104.0U
M75  702 702 1 1 npf L=2.0U W=2.0U
M76  1 701 701 1 npf L=2.0U W=2.0U
M77A 1 712 714 1 npf L=2.0U W=80.0U
M78  115 714 714 115 nnf L=2.0U W=4.0U
M79  713 714 1 115 nnf L=10.0U W=2.0U

* Stage 8
M81A 1 802 812 115 nnf L=2.0U W=36.0U
M82A 1 801 812 115 nnf L=2.0U W=36.0U
M83  802 103 800 115 nnf L=2.0U W=109.0U
M84  800 805 801 115 nnf L=2.0U W=109.0U
M85  802 802 1 1 npf L=2.0U W=2.0U
M86  1 801 801 1 npf L=2.0U W=2.0U
M87A 1 812 814 1 npf L=2.0U W=80.0U
M88  115 814 814 115 nnf L=2.0U W=4.0U
M89  813 814 1 115 nnf L=10.0U W=2.0U

* Stage 9
M91A 1 902 912 115 nnf L=2.0U W=36.0U
M92A 1 901 912 115 nnf L=2.0U W=36.0U
M93  902 103 900 115 nnf L=2.0U W=114.0U
```

```
M94   900 905 901 115 nnf L=2.0U W=114.0U
M95   902 902 1 1 npf L=2.0U W=2.0U
M96   1 901 901 1 npf L=2.0U W=2.0U
M97A  1 912 914 1 npf L=2.0U W=80.0U
M98   115 914 914 115 nnf L=2.0U W=40U
M99   913 914 1 115 nnf L=10.0U W=2.0U


* OP Amp circuit
M1001 126 127 122 115 nnf L=10.0U W=40.0U
M1002 122 0 125 115 nnf L=10.0U W=40.0U
M1003 126 126 128 1 npf L=22.0U W=10.0U
M1004 128 126 125 1 npf L=22.0U W=10.0U
M1005 129 125 128 1 npf L=10.0U W=45.0U
M1006 124 123 129 115 nnf L=10.0U W=10.0U
M1007 122 123 124 115 nnf L=50.0U W=10.0U
M1008 124 123 123 115 nnf L=10.0U W=10.0U

*Op amp Resistors and capacitor
Rbias 128 123 2K
Rf   127 129 20K
Rz   125 999 13K
Cc 999 129 5pF

* Final voltage shifter
M1009 128 129 130 1 npf L=2.0U W=10.0U
M1010 124 130 130 115 nnf L=2.0U W=4.0U

****Simulation Parameters********
.option dcon=1 probe
.print V(130)
.tran 333333ns .1s
.end
```

C. MOD 7 FOLDING CIRCUIT

```
** mod7f6.sp
** This file implements a mod 7, 6 stage folding corcuit
** SPICE file created for 5.0 volt circuit analogtest
** Technology: scmos

.MODEL nnf NMOS(LEVEL=2 VTO=+0.75 TOX=400E-10
+ NSUB=8.0E+15 XJ=0.15U LD=0.20U U0=650 UCRIT=0.62E5
+ UEXP=0.125 VMAX=5.1E4 NEFF=4.0 DELTA=1.4 RSH=36
+ CGSO=1.95E-10 CGDO=1.95E-10 CJ=195U CJSW=500P MJ=0.76
+ MJSW=0.30 PB=0.8 PHI=0.6 GAMMA=0.5 LAMBDA=0.0667
+ KP=10.0e-5)

.MODEL npf PMOS(LEVEL=2 VTO=-0.75 TOX=400E-10
+ NSUB=6.0E+15 XJ=0.05U LD=0.20U U0=255 UCRIT=0.86E5
+ UEXP=0.29 VMAX=3.0E4 NEFF=2.65 DELTA=1.0 RSH=101
+ CGSO=1.9E-10 CGDO=1.9E-10 CJ=250U CJSW=350P MJ=0.535
+ MJSW=0.34 PB=0.8 PHI=0.6 GAMMA=0.5 LAMBDA=-0.1
+ KP=4.0e-5)


** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 103 = Vin
** NODE: 115 = Vss
** NODE: 130 = Vout

*Input signal
Vin 103 0 PWL 0 0.0V, 0.1s 3.0V

*Sources
Vdd  1   0  5V
Vss  115 0 -5V
Vop+ 128 0  5V
Vop- 124 0 -5V

* Reference voltages for folds
* Vref1 = 0.0v
Vref2 205 0 0.656V
Vref3 305 0 1.312V
Vref4 405 0 1.968V
Vref5 505 0 2.624
Vref6 605 0 3.28

*Current sources
I11 112 115 .1ma
I21 100 115 .1ma
```

```
I12 212 115 .1ma
I22 200 115 .1ma
I13 312 115 .1ma
I23 300 115 .1ma
I14 412 115 .1ma
I24 400 115 .1ma
I15 512 115 .1ma
I25 500 115 .1ma
I16 612 115 .1ma
I26 600 115 .1ma

* Input resistors for summing amplifier
R1 113 127 1K
R2 213 127 1K
R3 313 127 1K
R4 413 127 1K
R5 513 127 1K
R6 613 127 1K

** Folding stages
* Stage 1
M11A 1 102 112 115 nnf L=2.0U W=36.0U
M12A 1 101 112 115 nnf L=2.0U W=36.0U
M13  102 103 100 115 nnf L=2.0U W=28.0U
M14  100 0 101 115 nnf L=2.0U W=28.0U
M15  102 102 1 1 npf L=2.0U W=2.0U
M16  1 101 101 1 npf L=2.0U W=2.0U
M17A 1 112 114 1 npf L=2.0U W=80.0U
M18  115 114 114 115 nnf L=2.0U W=4.0U
M19  113 114 1 115 nnf L=10.0U W=2.0U

* Stage 2
M21A 1 202 212 115 nnf L=2.0U W=36.0U
M22A 1 201 212 115 nnf L=2.0U W=36.0U
M23  202 103 200 115 nnf L=2.0U W=29.0U
M24  200 205 201 115 nnf L=2.0U W=29.0U
M25  202 202 1 1 npf L=2.0U W=2.0U
M26  1 201 201 1 npf L=2.0U W=2.0U
M27A 1 212 214 1 npf L=2.0U W=80.0U
M28  115 214 214 115 nnf L=2.0U W=4.0U
M29  213 214 1 115 nnf L=10.0U W=2.0U

* Stage 3
M31A 1 302 312 115 nnf L=2.0U W=36.0U
M32A 1 301 312 115 nnf L=2.0U W=36.0U
M33  302 103 300 115 nnf L=2.0U W=31.0U
M34  300 305 301 115 nnf L=2.0U W=31.0U
M35  302 302 1 1 npf L=2.0U W=2.0U
```

```
M36  1 301 301 1 npf L=2.0U W=2.0U
M37A 1 312 314 1 npf L=2.0U W=80.0U
M38  115 314 314 115 nnf L=2.0U W=4.0U
M39  313 314 1 115 nnf L=10.0U W=2.0U

* Stage 4
M41A 1 402 412 115 nnf L=2.0U W=36.0U
M42A 1 401 412 115 nnf L=2.0U W=36.0U
M43  402 103 400 115 nnf L=2.0U W=32.0U
M44  400 405 401 115 nnf L=2.0U W=32.0U
M45  402 402 1 1 npf L=2.0U W=2.0U
M46  1 401 401 1 npf L=2.0U W=2.0U
M47A 1 412 414 1 npf L=2.0U W=80.0U
M48  115 414 414 115 nnf L=2.0U W=4.0U
M49  413 414 1 115 nnf L=10.0U W=2.0U

* Stage 5
M51A 1 502 512 115 nnf L=2.0U W=36.0U
M52A 1 501 512 115 nnf L=2.0U W=36.0U
M53  502 103 500 115 nnf L=2.0U W=33.0U
M54  500 505 501 115 nnf L=2.0U W=33.0U
M55  502 502 1 1 npf L=2.0U W=2.0U
M56  1 501 501 1 npf L=2.0U W=2.0U
M57A 1 512 514 1 npf L=2.0U W=80.0U
M58  115 514 514 115 nnf L=2.0U W=4.0U
M59  513 514 1 115 nnf L=10.0U W=2.0U

* Stage 6
M61A 1 602 612 115 nnf L=2.0U W=36.0U
M62A 1 601 612 115 nnf L=2.0U W=36.0U
M63  602 103 600 115 nnf L=2.0U W=35.0U
M64  600 605 601 115 nnf L=2.0U W=35.0U
M65  602 602 1 1 npf L=2.0U W=2.0U
M66  1 601 601 1 npf L=2.0U W=2.0U
M67A 1 612 614 1 npf L=2.0U W=80.0U
M68  115 614 614 115 nnf L=2.0U W=4.0U
M69  613 614 1 115 nnf L=10.0U W=2.0U

* OP Amp circuit
M1001 126 127 122 115 nnf L=10.0U W=40.0U
M1002 122 0 125 115 nnf L=10.0U W=40.0U
M1003 126 126 128 1 npf L=22.0U W=10.0U
M1004 128 126 125 1 npf L=22.0U W=10.0U
M1005 129 125 128 1 npf L=10.0U W=45.0U
M1006 124 123 129 115 nnf L=10.0U W=10.0U
M1007 122 123 124 115 nnf L=50.0U W=10.0U
M1008 124 123 123 115 nnf L=10.0U W=10.0U
```

```
*Op amp Resistors and capacitor
Rbias 128 123 2K
Rf  127 129 20K
Rz  125 999 13K
Cc 999 129 5pF

* Final voltage shifter
M1009 128 129 130 1 npf L=2.0U W=10.0U
M1010 124 130 130 115 nnf L=2.0U W=4.0U


****Simulation Parameters********
.print V(103) V(130)

.option dcon=1 post
.tran 333333ns .1s
.end
```

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